Digitally Controlled Oscillator for WiMAX in 40 nm

Master's Thesis

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Digitally Controlled Oscillator for WiMAX in 40 nm

THESIS

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Digitally Controlled Oscillator for WiMAX in 40 nm

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Abstract

This document describes the design and implementation of a digitally controlled oscillator for WiMAX application in 40 nm. This system contains two main blocks of an LC oscillator with a digitally controlled capacitor bank and a frequency-dividing chain containing frequency dividers with different division ratios and a frequency doubler to cover two frequency bands of WiMAX.

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Preface

There were several important factors which made this project different than other student projects. I was fortunate enough to be accepted as a trainee at Catena Microelectronics BV. The time I spent there was both enjoyable and instructive. The Staff made my stay in Catena very comfortable with their warm welcome and patience towards my frequent questioning. I would like to thank Marcel van der Gevel without whom it was impossible to make daily progress. I would also like to thank Atze van der Goot, Koen van Hartingsveldt, Gerard Lassche, Suhaib Iqbal, Federico Bruccoleri and all the other engineers in Catena who supported me all the way. Most important of all, I would like to thank my daily Catena supervisor, Frank Verwaal, whose knowledge and wisdom were essential to the progress of this project.

I was fortunate enough to be a part of a team-project with two friends who helped and supported me everyday. I would like to thank Wenlong Jiang and Popong Effendrik with whom I share many wonderful memories during our stay in Catena.

I would also like to thank three of my best friends, Ali, Siamak and Nasir who helped me enormously in preparing this document with their technical support. I would also like to thank Siavash, Pejman, Nami and all my good friends who have been supporting me everyday.

At the end, I would like to thank my proffessor and supervisor, Dr. Robert Bogdan Staszewski who took me under his wings and introduced me to one of the most fascinating fields in RF design. His experience and knowledge guided me through this project from the beginning to the end and I am utterly grateful for his patience, kindness and support.

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Chapter 1

Introduction

Wireless communication has been of great interest for the last few decades. Scaling down of CMOS technology is providing many opportunities for RF designer to be able to achieve the highest levels of integration for system-on-chip. However, demand for high speed transceivers is also growing by the birth of numerous applications which makes the RF front-end design more challenging than ever. Although scaling-down technology is improving the computation capabilities of digital blocks, RF designer have to face more limitations such as low-voltage power supplies, degraded matching and low intrinsic gain of the devices. Despite of digital design process, robust RF design requires a thorough investigation of performance for different components in high frequencies under environmental and process variations.

One of the most important parts of a transceiver to be designed is the frequency synthesizer. *Phase Locked Loops* are the most common frequency synthesizer used in wireless technology. Figure 1 shows a charge-pump PLL which is widely used in frequency synthesizer design. Voltage controlled oscillator is one the most important parts of the charge-pump PLL which generates the high frequency clock. The frequency-divided clock is fed back to the PLL loop and compared with the reference clock *FREF*. The time difference between these two clock signals is detected by the phase/frequency detector *PDF* and a pulse is generated which controls the current sources in the charge pump. The output of the charge pump is then fed to a loop filter which generates a tuning voltage which controls the frequency of the VCO. The closed-loop PLL will bring the frequency of the VCO to be N times the reference clock frequency.

A voltage controlled oscillator is a tunable RF block whose output frequency is determined by a control voltage. Two important specifications determine the frequency-related capabilities of a VCO: frequency resolution and tuning range. As it will be discussed in detail in the next chapter, these two specifications often contradict each other in terms of design parameters and optimization.

The charge pump circuitry in traditional PLLs is both power and area consuming. Regarding the scaling-down technology whose main goal is increase computation capabilities

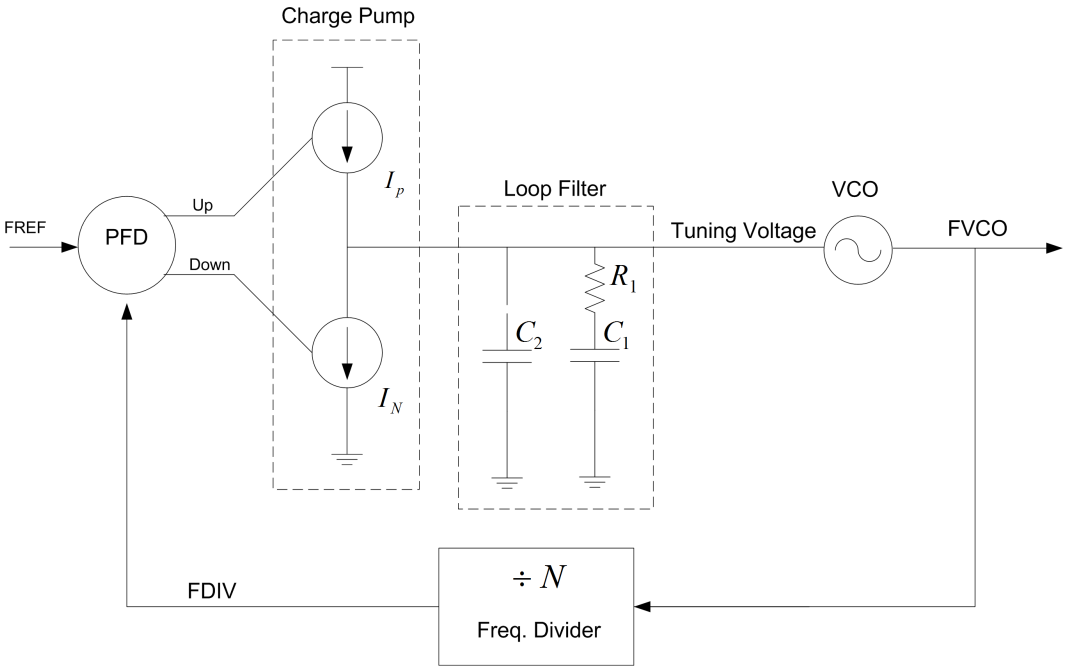

Figure 1.1: Charge pump phase-locked loop architecture [11], [21].

per area unit, an *All-Digital PLL* is has shown to be a successful approach in designing low-power low-area frequency synthesizers in new technologies. ADPLL has the minimum number of RF blocks and is more taking advantage of the digital capabilities of the new technologies which can improve system performance. A simplified block diagram of an all-digital PLL is shown in figre 1.

Figure 1 shows some similarities with figure 1 in terms of input/output definition and system specifications, although system configuration is basically changed in an all-digital PLL. The VCO in a traditional PLL is replaced by a DCO: *digitally controlled oscillator*. The tuning voltage is the ADPLL are the *frequency command word*, FCW and the reference clock, f_{REF}. The oscillator phase accumulator determines the phase of the DCO output in one cycle of the reference clock. A *time-to-digital converter*, TDC, can compensate for the fractional phase error of oscillator phase accumulator. The phase detector then generates the phase error, PHE, which is fed to the loop filters to produce *normalized tuning word*, NTW. The *oscillator tuning word* (OTW) is obtained by multiplying NTW with the normalization ratio of f_R divided by $\hat{K}_{DCO}$ which is the DCO gain and is defined as the frequency change in the output of the DCO due to change of one LSB in the DCO tuning word.

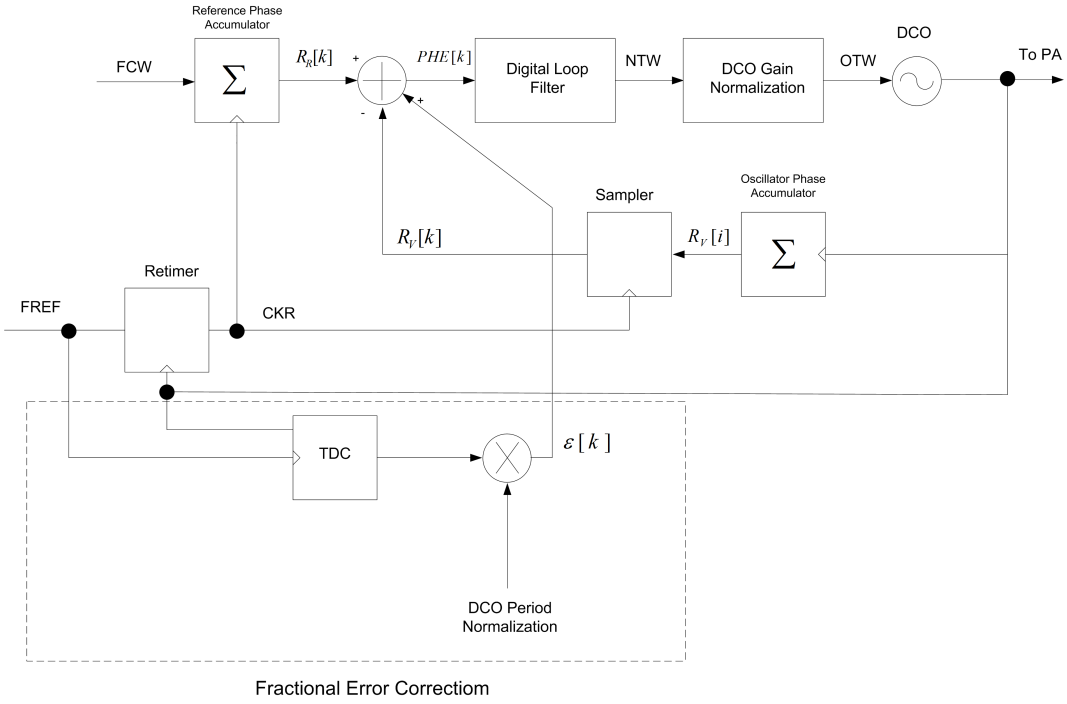

Figure 1.2: All-digital phase-locked loop architecture [11], [21].

Digitally Controlled Oscillator

The basic function of a digitally controlled oscillator is to generate a periodic signal whose frequency is digitally controlled by a control word. DCOs are widely designed and used for ADPLLs [23], [10], [5], [22]. There are several DCO topologies which can be used in an ADPLL. LC oscillators are among the most used oscillators in transceiver designs. The most important feature of the LC oscillators is the low phase noise. In all digital PLLs, the quantization noise introduced by the frequency discretization in the digitally controlled oscillator can affect the performance in terms of out-of-band phase noise [5]. The most important part of a DCO is the capacitor bank. The capacitor bank consists of two or more groups of varactors with different specifications. The capacitor bank can provide the DCO with coarse and fine frequency steps. Therefore, the tuning range and frequency resolution of a DCO are defined by the use of different varactors. Varactors are variable capacitance which are controlled by a tuning voltage in case of VCOs and control bit in case of DCOs.

At high frequency operations, the parasitics and losses of the varactor determine the performance of the capacitor bank and the DCO. In chapter 2 different parts of the DCO are introduced and described in detail.

According to the frequency planning introduced in chapter 2, A frequency dividing chain is needed for the DCO system to cover the required frequency bands of WiMAX.

Frequency dividers divide the frequency of the input signals by a certain ratio. The division ratios for different frequency dividers are also determined by frequency planning. In chapter 3, The design of different frequency dividers are described in detail and their performance is investigated.

Chapter 2

Digitally Controlled Oscillator Core

2.1 Introduction

The design of a digitally controlled LC oscillator is based on a series of specifications which is dictated by the ADPLL design. Tuning range, power consumption, frequency resolution and phase noise are among the most important specifications which determine the performance of the DCO and the ADPLL. Specific requirements on each parameter are based on the application for which this design is proposed. WiMAX application requirements mostly correspond to a low-power design whereas other applications where the noise performance of the oscillator has to meet stricter noise criteria like Bluetooth and GSM. In this chapter these requirements are introduced. According to these requirements, a design approach is introduced and described in details in the following sections.

In this chapter, the frequency planning of the total DCO system is presented which can be directly used in an all-digital PLL. The circuit basic functionality and the enhancing modifications which are required for different requirements are described. The most important part of the DCO design is dedicated towards the design of the capacitor bank. It is shown how the capacitor bank is directly affecting the DCO performance and how it is compromising the DCO output specifications. The capacitor bank contains of three major parts: PVT, $Acquisition$ and $Tracking$. Each part of the capacitor bank serves for a different purpose but their specifications are not independent from one another. Each part is described in detail in the following sections of this chapter.

2.2 Frequency Planning

According to WiMAX application requirements, the oscillator has to cover two frequency bands:

1. Low frequency band: 2.3 GHz - 2.7 GHz
2. High frequency band: 3.3 GHz - 3.8 GHz

There are several oscillator topologies which are candidates to be used as a DCO. Ring oscillators and LC oscillators are among the most popular topologies. According to the phase-noise and frequency tuning requirements, LC oscillator seems to be a better choice for this design. As it will be described later, in an LC oscillator with a single inductor, the capacitor bank is required to determine the oscillation frequency throughout the required frequency range.

In order to achieve low-power performance, a single core LC oscillator which contains only one inductor, is an interesting choice. The most challenging part of designing a single core LC oscillator is to build a capacitor bank which can cover both frequency bands of interest.

In a digitally controlled oscillator, the capacitor bank is made of digitally controlled varactors. In contrast with traditional VCO where a tuning voltage is applied to a varactor which determines its capacitance value, a tuning bit is applied to a digitally-controlled varactor in a DCO which determines the capacitive mode of the varactor. Each capacitive mode corresponds to a capacitance value. Three different varactor (capacitor) banks with different configurations are used in this design which are described in detail in 2.5. The total capacitance of the varactor bank in any state of the tuning word combined with the fixed value of the on-chip spiral inductor will determine the output frequency of the DCO using equation 2.1.

$$f_{oc} = \frac{1}{2\pi\sqrt{LC}} \tag{2.1}$$

Where C is the total capacitance value of the capacitor bank and L is value of the inductor. In order to cover both frequency bands using only a single core LC oscillator, two different approaches can be made:

1. Switched inductor: It is possible to design a switching inductor to be used in this design. The switching inductor can bypass one or more turns of the spiral inductor in order to bring the frequency range provided by the capacitor bank to the high-frequency band and vice versa. The most important drawback of this topology is the degradation imposed on the quality factor of the inductor because of the switch which is placed close to the silicon as opposed to the inductor metal which is placed on top.

2. Frequency Divider: If the DCO is followed by two different frequency dividing paths with different division ratios, a single core DCO can cover two frequency bands simultaneously.

The use of frequency dividers seem be to a reasonable approach in terms of relaxing the tuning range requirements of the capacitor bank. In order to understand how it works, two different approaches are compared with each other:

- The frequency tuning range is covered by using varactors only: The total frequency range is 2.3 GHz to 3.8 GHz. this results in a tuning range of %65 (see equation 2.12).
- The frequency tuning range is covered by dividers: In order to use frequency-dividing paths to cover both frequency bands, the intrinsic frequency of the DCO has to be higher than the previous approach. In order to find the division ratios and the required DCO frequency range, a set of multiplying factors must be applied to each frequency band to bring both bands into two similar frequency ranges which are mostly overlapping. In this case multiplying factor of 2 and 3 are chosen for the high-band and the low-band respectively:
- $[2.3\ GHz, 2.7\ GHz] \times 3 = [6.9\ GHz, 8.1\ GHz]$
- $[3.3\ GHz, 3.8\ GHz] \times 2 = [6.6\ GHz, 7.6\ GHz]$

The resulting frequency bands are fairly overlapping and by combining both bands the frequency range of the proposed DCO can be calculated as $[6.6\ GHz, 8.1\ GHz]$. The tuning range of this DCO is %23 which is much smaller than the tuning range calculated in the topology without dividers. This architecture is shown as a block diagram in figure 2.1.

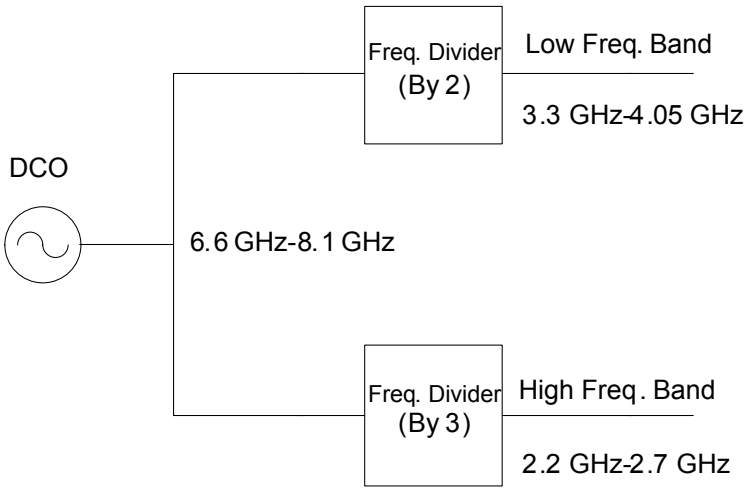

Figure 2.1: Block diagram of the initial DCO architecture using frequency dividers.

Parallel dividing paths help to relax the tuning range specifications of the capacitor bank but the frequency dividers add to the total power consumption of the DCO system.

According to the specifications of the transceiver and the mixers in particular, the LO is required to generate quadrature signals. Quadrature signals consists of two in-phase (I) and quadrature-phase (Q) signals which have 90° phase shift. A single core oscillator used in this design is unable to produce such clock signals since only one inductor is used in the

LC tank and injection locking methods are not an option.

Another way to produce I/Q signals is to used frequency dividers. A divide-by-two frequency divider can use both the rising and falling edge of its differential input signal in order to generate differential I/Q signals with half of the input frequency. Therefore, it needs an input signal with %50 duty cycle. Any deviation from %50 will result in an I/Q phase error. In chapter 3, it is described in detail how these frequency dividers work and a complete circuit analysis is provided.

The low-band part of the DCO contains a dividing ratio of 3. Traditional divide-by-3 frequency dividers are based on D flip-flop design. In order to generate I/Q outputs, divide-by-3 frequency dividers require I/Q differential signals as their input. Since the DCO core cannot provide I/Q signals for such frequency division, a divide-by-two frequency divider has to be placed before or after the divide-by-3 frequency divider to generate quadrature outputs. This will bring the low-band output frequency to half of the desired value. A frequency doubler can be used to compensate for the excessive frequency division. Digital frequency doublers which are more adaptable to this design require I/Q input signals which can be provided by the divide-by-3 frequency divider. However, the output of such frequency doubler is only differential and does not contain quadrature phase which is needed for the transceiver. In order to solve this problem, the DCO frequency range can be doubled. This will also double the frequency division ratios in both high-band and low-band of the divider chain.

By doubling the frequency range of the DCO, new division ratios for the dividing paths can be calculated as before:

- $[2.3\ GHz, 2.7\ GHz] \times 6 = [13.8\ GHz, 16.2\ GHz]$
- $[3.3\ GHz, 3.8\ GHz] \times 4 = [13.2\ GHz, 15.2\ GHz]$

The final tuning range for the DCO core in this case is $[13.2\ GHz, 16.2\ GHz]$. As it will be described in section 2.5, PVT varactor bank responsibility is to provide this tuning range for the DCO with large frequency resolution. Process, voltage and temperature variations require a certain margin for this tuning range to make sure that all frequencies are covered in both frequency bands. Initial simulations indicate that 1.5 GHz margin is required on both sides of the DCO tuning range, bringing it to $[11.7\ GHz, 17.7\ GHz]$. Figure 2.2 shows how the high frequency and the low frequency bands are covered by different division rations.

Another advantage of doubling the DCO core frequency is the layout considerations for the whole transceiver. In some cases, the LO signals have travel through the chip to reach the rest of the transceiver. Different kinds of pipes are used to transfer the LO signals. The long routing of the pipe might result in I/Q phase error if quadrature phases are both transformed. To avoid such errors, It is possible to place the final divide-by-2 frequency divider as close to the transceiver as possible. This will allow transferring only one of the

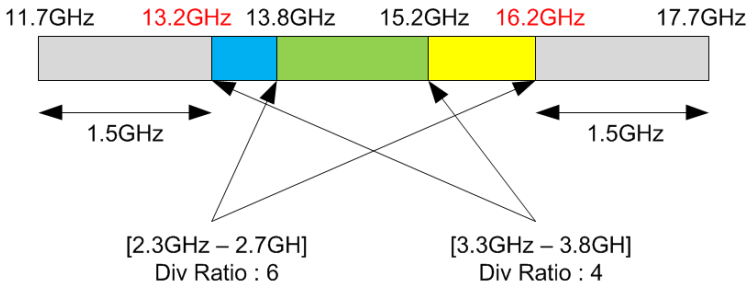

Figure 2.2: DCO frequency range covers both high and low frequency bands with division rations of 4 and 6 respectively.

differential phases. This will determine the final architecture of the divider chain:

- High frequency band: the division ratio is 4. Two divide-by-2 frequency dividers can be used to provide this division ration. The second divider can be placed after the pipe.
- Low frequency band: the division ratio is 6. First frequency division can be shared by the high-band first divider. Quadrature signals are available to place a divide-by-3 frequency divider which produces I/Q signals. Since the division ratio is completed at this point, a frequency doubler is used after the divide-by-3 frequency divider to compensate for the final frequency division. The quadrature outputs of the divide-by-3 frequency divider allow the frequency doubler to be implemented in a digital configuration which generates differential outputs with twice the frequency.

The final architecture of the DCO system is shown in figure 2.3.

A small divide-by-2 frequency doubler is used in the feedback to drive a phase rotator. The output of the phase rotator is then fed to the ADPLL main loop.

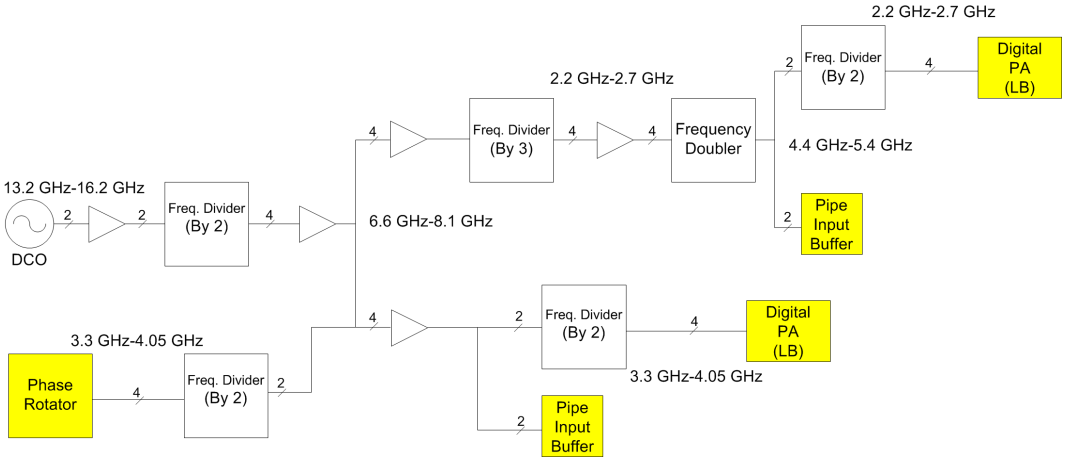

Figure 2.3: DCO system architecture according to the frequency planning.

2.3 DCO Core Topology

The schematic of the DCO core is shown in figure 2.4.

The LC oscillator shown in figure 2.4 is a differential pull-up pull-down topology [7], [8]. Two set of cross-coupled PMOS and NMOS transistors are used to create negative *gm* in order to compensate for the losses in the LC tank. This is the essential condition under which oscillation takes place. In a small signal model shown in figure 2.5.

The total losses in the LC tank are modeled with a resistor parallel to the tank. The total negative *gm* provided by the cross-coupled transistors are also modeled with another branch which is also parallel to the tank. Equation 2.2 indicated the oscillation condition in terms of R_{loss} and *gm*:

$$gm \geq \frac{1}{R_{loss}} \tag{2.2}$$

The desired frequency is filtered within the LC tank the differential output start building up until the nonlinearities of the circuit affect the negative *gm* and the output oscillation amplitude comes to constant value. These nonlinearities exist in the cross-coupled transistors. When output amplitude starts to increase, so does the drain voltage of the cross-coupled transistors and they are driven more into the triode region. This will limit the effective *gm* of the cross-coupled pair and at some point the amplitude stops to increase and the output voltage swings becomes constant. By increasing the width of these transistors, larger *gm* can be achieved to compensate the tank loss and improve the DCO output phase noise.

Two resistive parts of the DCO core are as follows:

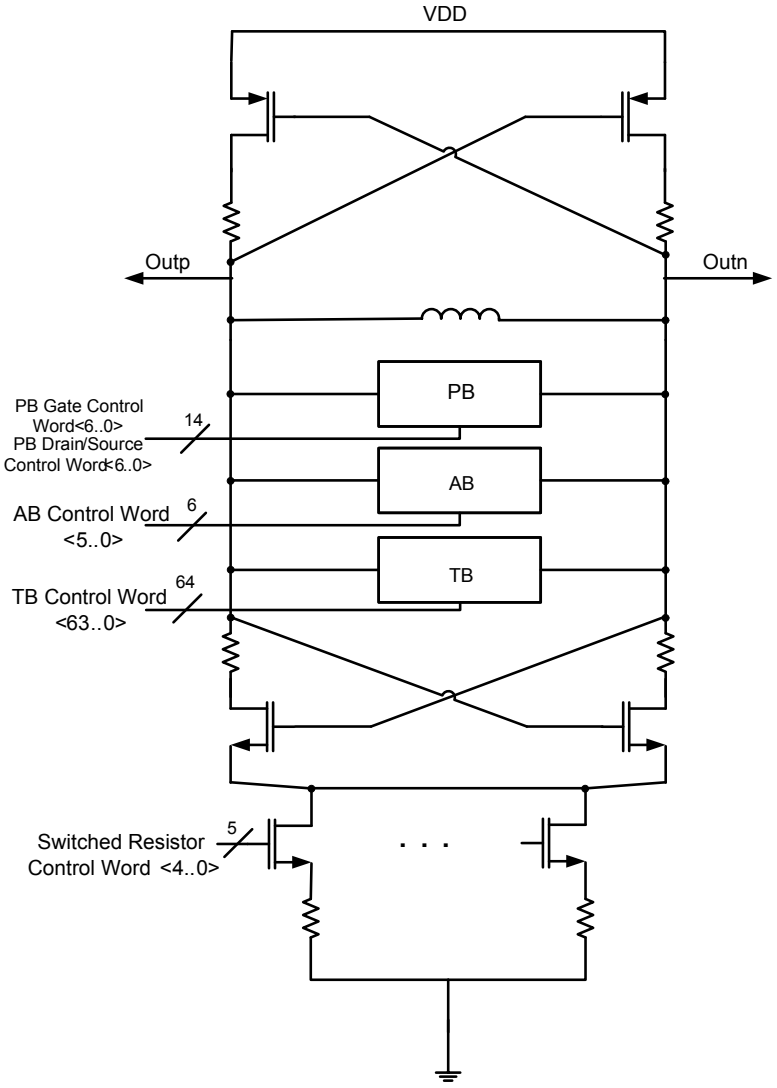

Figure 2.4: DCO core with a differential pull-up pull-down topology.

- Degenerative resistors: as it is shown in the schematic of the DCO core in figure 2.4, a resistor added to the drain of each transistor in the cross-coupled pairs. As shown in figure 2.6, This resistor increases the ON-resistance of the transistors which makes the resonator Q less sensitive to any r_{on} modulation. This will effectively improve the up-converted $1/f$ noise i.e. the -30 dB/dec region of the output phase noise [13]. The most important drawback of this topology is the effect of the resistance thermal noise on the -20dB slope part of the phase noise which is not considerable.

- Switched tail resistors: due to the low typical voltage of the power supply in this technology and also the low output impedance of the devices, tail current mirrors in conventional oscillators is replaced by switched tail resistors. Five binary-weighted

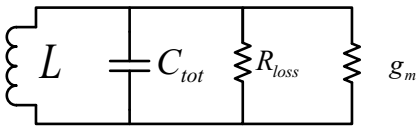

Figure 2.5: Small Signal model of the LC tank, its loss and the negative *gm*.

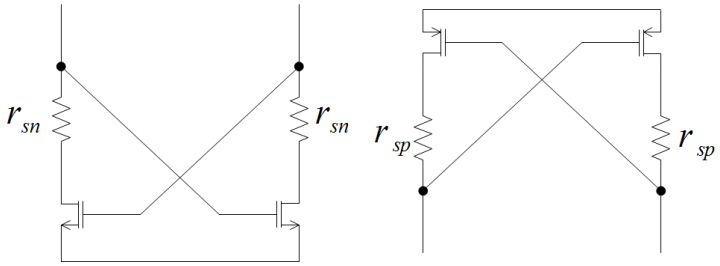

Figure 2.6: The degenerative topology of the cross-coupled pairs: r_{sn} and r_{sp} are added to the cross-coupled transistors of figure 2.4 improve the phase noise in the up-converted $1/f$ region.

switched resistors are used in this DCO which are controlled by a 5-bit binary controlled word. The current consumption of the DCO can be modified in different frequencies and different process corners using these switched resistors.

2.4 Inductor

A symmetric spiral inductor is used in this design. The value of the inductor can be determined to adjust the tuning range of the DCO and bring it to the required DCO frequency band.

A two-turn inductor can be found in the available components provided by the 40 nm technology. The upper thick metals are used to implement the inductor which results in low series resistance of the inductor (metal 6 and 7). Quality Factor is important parameter which is defined to show the performance quality of the RF passive components in terms of their losses. The quality factor of a complex impedance is defined as in equation 2.3.

$$Q = \frac{imag(Z)}{real(Z)} \tag{2.3}$$

In equation 2.3 it is possible to substitute Z with a complex admittance. In the case of an inductor, the metal resistance in the inductor is modeled by a series resistance. The impedance of the inductor can then be expressed as in equation 2.4.

$$Z_L = r_s + j\omega L \tag{2.4}$$

The quality factor of the inductor can be expressed using equation 2.5.

$$Q_L = \frac{\omega L}{r_s} \tag{2.5}$$

Equation 2.5 shows how the thick metal's low resistance help improve the quality factor of the inductor because r_s is reduced. However, the actual model of the inductor is much more complex than just a series resistor and inductor. Numerous capacitive and resistive parasitic exist between the three terminals of the inductor (two main terminals and one bulk connection).

In figure 2.7, The quality factor of the inductor is shown as a function of frequency. The peak of the Q-plot indicates the optimum frequency range in which the inductor can deliver high quality performance in terms of losses.

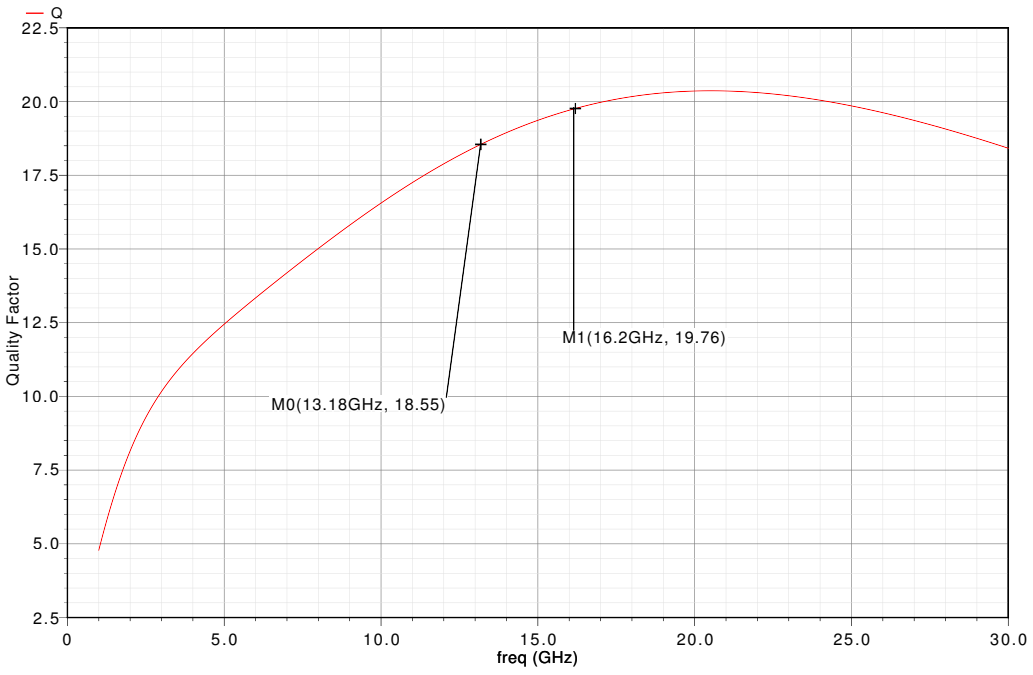

Figure 2.7: Spiral inductor quality factor.

The inductor value and its quality factor are plotted versus frequency for different process corners in figure 2.8.

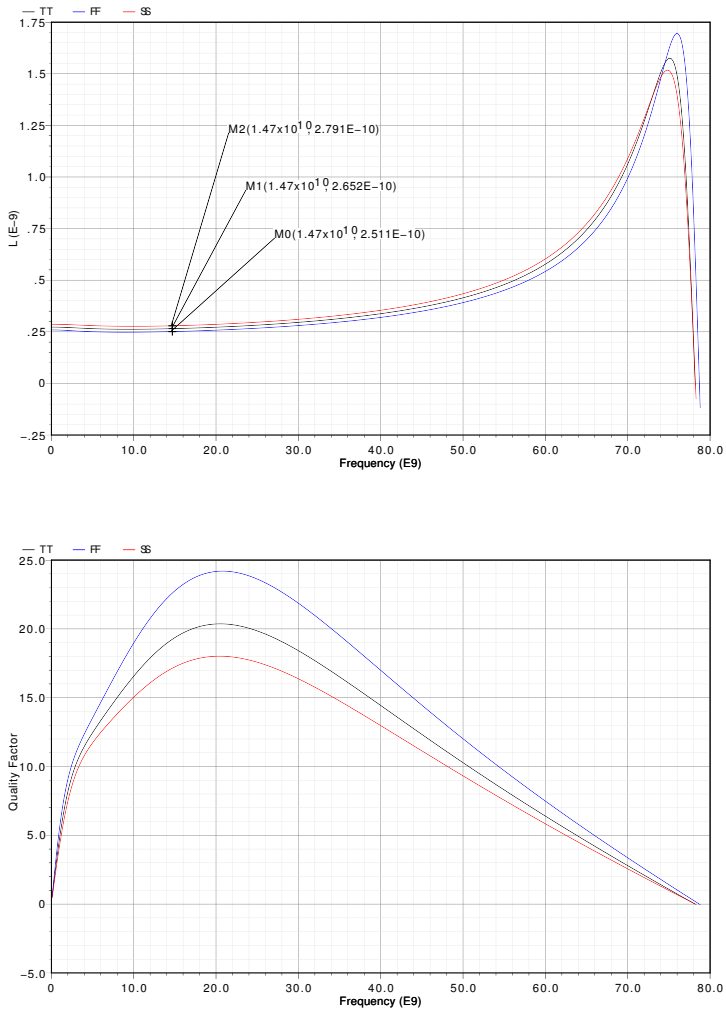

Figure 2.8: L and Q plots of the spiral inductor in typical (TT), fast (FF) and slow (SS) process corners.

It can be seen that the value of the inductor is slightly changed in different corners. Quality factor peak is also influenced, but the peak frequency stays the same. The inductor value variation is quite small in the desired frequency band.

2.5 Capacitor Bank

2.5.1 Introduction

The specified frequency range for DCO is covered using varactors. Varactors are variable capacitors whose capacitance is a function of the voltage applied to it. In a digitally controlled oscillator, digitally controlled varactors are used. A two-level control voltage is applied to the varactor which determines varactor cap-mode: high-capacitance mode and low-capacitance mode. This control bit toggles between the lowest and highest power supply voltages which are 1.2V and 0V in this case. When the control bit is high, varactor is in the high-capacitance mode and when the control bit is low, varactor is in the low-capacitance mode. Capacitance values in each mode are related to each other by equation 2.6:

$$C_{k,on} = C_{k,off} + \Delta C_k \tag{2.6}$$

where $C_{k,on}$ (C_{max}) and $C_{k,off}$ (C_{min}) are the varactor capacitance value in the high-capacitance mode (ON state) and the low-capacitance mode (OFF state) of the varactor respectively. Total capacitance of the varactor can then be derived using 2.7:

$$C_k = C_{k,off} + d_k \times \Delta C_k \tag{2.7}$$

where d_k indicates the digital value of the control bit which is 1 for the ON state and 0 for the OFF state. ΔC_k is the capacitance step that a varactor can provide. There are two different design specifications which require two different approaches to varactor design: *tuning range* and *frequency resolution*.

Tuning Range

The varactors are responsible to cover a certain frequency range that is assigned to the DCO. This frequency tuning range is determined according to the frequency planning. varactors variable capacitances provide this tuning range. Suppose there are n parallel varactors in the LC tank as depicted in figure 2.9. Total capacitance of the bank can then be calculated using equation 2.8.

$$C_{total} = \sum_{k=1}^{n} C_k = \sum_{k=1}^{n} (C_{k,off} + d_k \times \Delta C_k) \tag{2.8}$$

According to 2.1, the highest frequency of the DCO is achieved when all the varactors are in their OFF state, i.e. low-capacitance mode, whereas the lowest frequency of the DCO is achieved when all varactors are in their ON state, i.e. high-capacitance mode. So 2.1 can be rewritten as in equation 2.9.

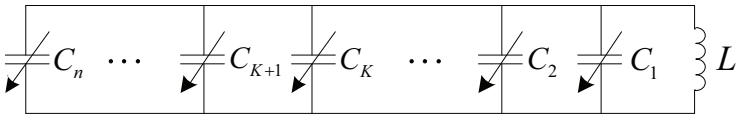

Figure 2.9: LC tank of a digitally controlled oscillator.

$$f = \frac{1}{2\pi\sqrt{L\sum_{k=1}^{n}(C_{k,off} + d_k \times \Delta C_k)}} \tag{2.9}$$

$$\Delta C_{tot} = \sum_{k=1}^{n} \Delta C_k \tag{2.10}$$

$$C_{tot,off} = \sum_{k=1}^{n} C_{k,off} \tag{2.11}$$

According to equation 2.10, the largest possible capacitance change of the varactor bank is the sum of all the varactors' capacitance steps. Varactors with large capacitance step (ΔC) result in larger ΔC_{tot}. Tuning range is defined as in equation 2.12:

$$TR = \frac{f_{max}}{f_{min}} - 1 \tag{2.12}$$

where f_{max} and f_{min} are the highest and lowest frequency of the DCO, respectively. f_{max} is achieved when all varactors are in OFF state, whereas f_{min} is achieved when all varactors are in ON state. By substituting 2.9 in 2.12

$$\frac{f_{max}}{f_{min}} = \frac{\frac{1}{2\pi\sqrt{LC_{tot,off}}}}{\frac{1}{2\pi\sqrt{L(C_{tot,off}+\Delta C_{tot})}}} = \sqrt{1 + \frac{\Delta C_{tot}}{C_{tot,off}}} \tag{2.13}$$

It can be seen that tuning range can be improved by increasing ΔC_{tot}. This can be done by either increasing the number of varactors or by increasing the capacitance step (ΔC) of each varactor. Former solution has the major drawback of reducing the maximum achievable frequency by the DCO since increasing the number of varactors will also increase the total OFF state capacitance of the bank and decrease DCO maximum frequency according to equation 2.9 as well as the tuning range according to equation 2.13.

The other solution is to increase the capacitance steps of the varactors. As shown in equation 2.14, in order to increase ΔC, C_{max}/C_{min} have to increase. As mentioned before, C_{max} is the ON state capacitance and C_{min} is the OFF state capacitance of the varactor.

$$\frac{\Delta C}{C_{min}} = \frac{C_{max} - C_{min}}{C_{min}} = \frac{C_{max}}{C_{min}} - 1 \tag{2.14}$$

C_{max}/C_{min} ratio is a proper indicator of the varactors capability to meet the frequency range specification of the DCO. A simple model for a digitally controlled varactor is shown in figure 2.10. Basically it is a switched capacitor which is controlled by the control bit applied to the switch. When the control bit is high, the switch is conducting and the capacitor is in parallel with the tank. When the control bit is low, the switch is not conducting. Considering ideal components, in this case the impedance of the varactor seen by the tank is infinite i.e. $C_{min}(C_{off}) = 0$. But, as it will be explained in details in section 2.5.3, both the capacitor and the switch contain parasitics which will determine the OFF-state capacitance (C_{off}) of the varactor. So in the ON state, varactor capacitance is determined by the value of the varactor capacitor (C_v in figure 2.10) and in the off-mode, varactor capacitance is determined by the parasitics of the varactor. By lowering the parasitics, higher $\frac{C_{max}}{C_{min}}$ ratio can be achieved. This will lead to higher tuning range. So $\frac{C_{max}}{C_{min}}$ ratio of a varactor plays an important role in determining the tuning range of a DCO.

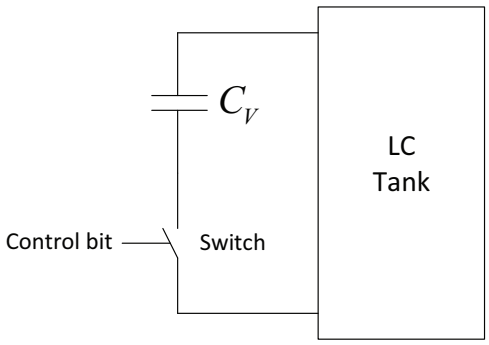

Figure 2.10: Switched-capacitor used as a digitally controlled varactor.

Frequency Resolution

An important factor in DCO performance is frequency resolution. Frequency resolution is the finest frequency step that DCO can deliver. It can be shown that in order to have smaller frequency steps i.e. better frequency resolution, ΔC of the varactors should become smaller. Equation 2.15 shows the relation between the capacitance step of the varactors and its according frequency step. This equation is derived by differentiating equation 2.1 in respect to C.

$$\frac{df}{f} = \frac{dC}{2C} \tag{2.15}$$

This specification for ΔC is in contrary with what was discussed in section 2.5.1. This means in order to meet frequency resolution specification, more number of varactors with less ΔC are required in order to maintain tuning range. This approach will have the follow-

ing consequences:

1. Increasing the number of varactors will introduce more parasitics ($C_{tot,off}$) to the tank. Since these parasitics determine the highest frequency of the DCO, f_{max} is reduced.

2. As the number of varactors grows, matching and linearity of the DCO become more challenging.

3. Each varactor needs a control bit. More varactors means more control bits which is not desirable due to routing complexity and top-level layout restrictions.

In order to solve this problem, two different varactors with different characteristics are introduced:

1. Varactor with high $\frac{C_{max}}{C_{min}}$ ratio in order to provide enough tuning range to cover the desired frequency bands. The frequency step of this varactor is usually much higher than DCO frequency resolution.

2. varactor with small ΔC which provides DCO with the desired frequency resolution but the capacitance step is much smaller than the parasitics which brings $\frac{C_{max}}{C_{min}}$ ratio of this varactor down and close to 1.

These two varactors will form 3 varactor banks each of which will be used through three major operational modes with progressively lower frequency range and higher resolution:

1. PVT bank: This bank consists of varactors with large frequency steps and has low frequency resolution. These varactors are responsible to cover the whole frequency range of the DCO according to frequency planning and also compensate for process and environmental variations which affect the output frequency of the DCO. This bank is calibrated during the first mode of operation.

2. Tracking bank: This bank consists of varactors with small frequency steps and high frequency resolution. These varactors are responsible to provide the desired frequency resolution. This dynamic part of the LC tank can be used to track the frequency reference and to perform data modulation. This bank corresponds to the last mode of operation.

3. Acquisition bank: This is an intermediate bank with medium-size frequency steps and medium frequency resolution. The varactors used in this bank are similar to those used in PVT bank, but they have lower frequency range and higher resolution. This bank corresponds to the second mode of operation.

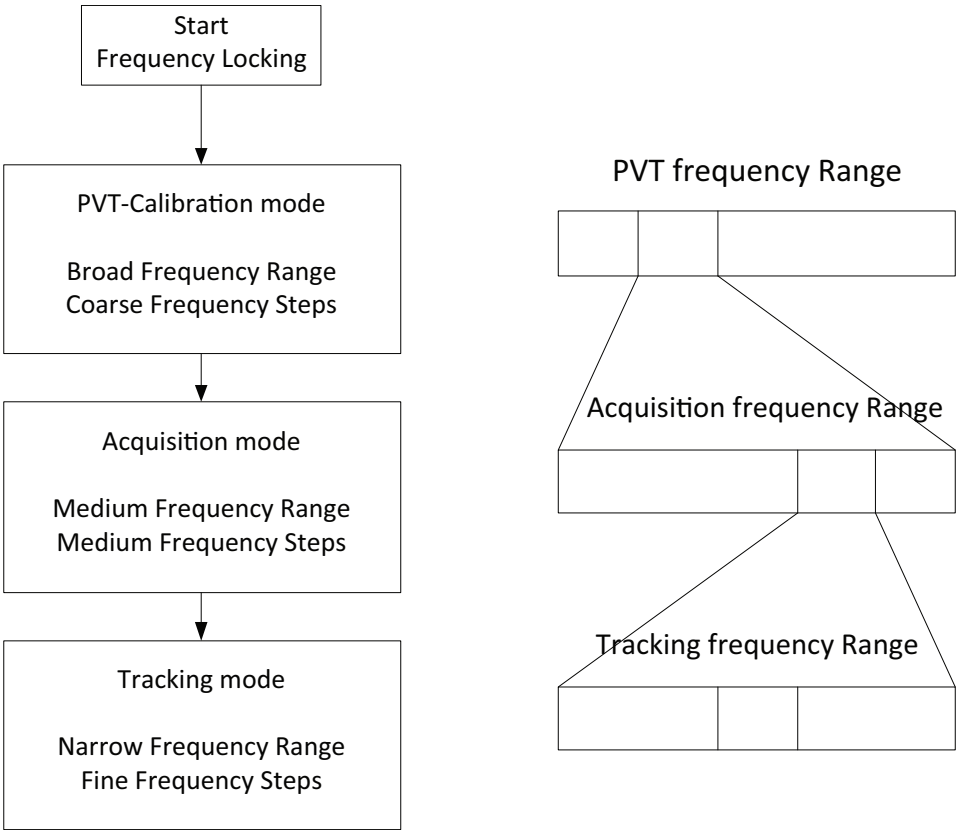

Figure 2.11: Three operational modes of DCO capacitor bank.

The operational modes are briefly described in chapter 1. A more visual way on how these three varactor banks are related to each other is depicted in figure 2.11.

As mentioned before, there are two important frequency specifications regarding each bank: total frequency range and frequency resolution. Assuming a constant value for L, DCO frequency range and frequency resolution correspond to PVT bank frequency range and Tracking bank frequency resolution respectively. This is clear according to the purpose of each bank as described before. The remaining specifications of the varactor banks can be set according to an important criterion. There is a relation between the frequency resolution of one bank with frequency range of the next bank corresponding to the next mode of operation. Ideally one might assume that it is sufficient that these two values are equal. In practice, a certain factor between these two values is considered to make sure that no range of frequency is missed. This consideration is due to certain nonlinearities which exists within each bank. This will be discussed in details in section 2.5.2.

Before going into detail about the characteristics of each bank, it is important to introduce binary weighted varactors. As mentioned earlier, each varactor mode is determined by

a control bit. Assume N varactors are needed for a bank. Hence, N control bits are required to control them and $N+1$ varactor states can be achieved. Using binary weighted varactors the number of varactors are reduced to $n = \log_2 N$. PVT and Acquisition bank varactors are implemented with binary varactors. The capacitance of PVT and acquisition banks can be calculated using equations 2.16 and 2.17.

$$C_{tot,P} = C^{P}_{tot,off} + \sum_{k=1}^{n_p} d^{p}_{k}(\Delta C_P.2^k) \tag{2.16}$$

$$C_{tot,A} = C^{A}_{tot,off} + \sum_{k=1}^{n_A} d^{A}_{k}(\Delta C_A.2^k) \tag{2.17}$$

where ΔC_P and ΔC_A are the capacitance steps of PVT and acquisition bank respectively which also correspond to the frequency step of the least significant bit. n_P and n_A are the number of bits in each bank. It is important to note that it is the varactors' ΔC that are weighted in a binary format, not the on-mode or off-mode capacitance. As is shown in equations 2.16 and 2.17, total capacitance of each bank when all the control bits are zero, determines the minimum capacitance value of the bank i.e. $C_{tot,off}$. Figure 2.12 illustrates how these varactors contribute to the total capacitance of the tank.

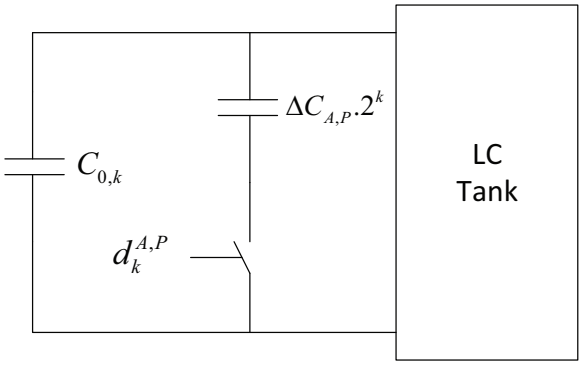

Figure 2.12: Capacitance contribution of a varactor to the LC tank.

Tracking bank is not implemented with binary weighted varactors. The reason is discussed in detail in section 2.5.6

2.5.2 Capacitor Banks

In order to design the LC tank, first all the undefined variables must be determined. These variables are related to each other according to pre-determined design specifications. This results in a set of equations where the number of variables exceeds the number of equations.

By going through some iterations and considerations, it is possible to find an optimal solution or at least close to optimal. These variables are as follows:

1. PVT bank:
   - $C^{P}_{tot,off}$: total OFF-state capacitance
   - ΔC_P: Capacitance step (frequency resolution)
   - n_P: number of varactors (control bits)
2. Acquisition bank
   - $C^{A}_{tot,off}$: total OFF-state capacitance
   - ΔC_A: Capacitance step (frequency resolution)
   - n_A: number of varactors (control bits)
3. Tracking bank
   - $C^{T}_{tot,off}$: total OFF-state capacitance
   - ΔC_T: Capacitance step (frequency resolution)
   - n_T: number of varactors (control bits)
4. Inductor

Some of these variables are related directly to DCO specifications as follows:

- As mentioned before, tracking bank varactors are designed in such a way that they provide high frequency resolution for the DCO. These varactors are then responsible to meet frequency resolution specification of the DCO. Fortunately this variable can be treated almost independently as shown in equation 2.18

$$df = (2\pi^2 L f^3) dc \tag{2.18}$$

  This equation is derived by substituting $C = \frac{1}{4\pi^2 f^2 L}$ from equation 2.1 into equation 2.15. It can be seen that in higher frequencies, lower capacitance step is needed to maintain frequency resolution. So as frequency increases, smaller capacitance step is required. This will determine tracking bank ΔC when $f = f_{max}$. The inductor value is not determined yet, but a reasonable estimation can help with equation 2.18. Any change in the estimated inductor value results in a minor error in ΔC_T which can be corrected within one iteration.

- As discussed in section 2.5.1, due to nonlinearity errors, there is always a margin factor between the frequency resolution ΔC of a bank with higher frequency range and total frequency range $(\Delta Ctot)$ of the next bank with lower frequency range. This factor can be shown using eqution 2.19.

$$\Delta C_{tot}^{i} = K_m.\Delta C^{i-1} \tag{2.19}$$

where i indicates the corresponding bank i.e. 1 for PVT bank, 2 for acquisition bank and 3 for tracking bank. K_m is the margin factor and can be reasonably estimated according to the nonlinearities. Initially this factor is set to 4. It will be shown later that this value is satisfactory. This relation between capacitance step and total capacitance variation of consecutive banks is shown in figure 2.13.

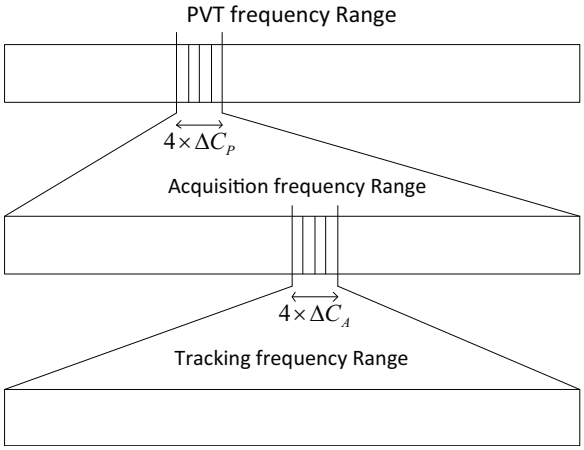

Figure 2.13: Relation between frequency resolution and frequency range of consecutive banks.

- The most dominant part of the tank that determines the frequency range of the DCO is PVT bank. As described before, PVT varactors are designed in order to have high frequency range and coarse frequency steps. So total capacitance change of the tank can be estimated with the total capacitance change of the PVT bank as shown in equation 2.20.

$$\Delta C_{tot} = \Delta C_{tot}^{P} \tag{2.20}$$

This is a useful approximation to determine the characteristics of the PVT bank.

By considering these three restrictions, all the ten variables of the tank can be found within a couple of iterations. It is important to note that these variables only indicate the

frequency-related properties of the tank components. There are other factors which determine the performance of the tank that must be taken into consideration. These important parameters require a considerate design for the varactors of each bank. These design procedures will be discussed in detail in the following sections of this chapter.

2.5.3 PVT Bank

In this section, PVT varactor design procedure, design challenges and solutions will be discussed in detail. As discussed before, the main purpose of PVT bank is to cover DCO desired frequency range with coarse frequency steps. Acquisition mode and Tracking mode will then provide better frequency resolution in the desired range. So varactors with high frequency range ($\frac{C_{max}}{C_{min}}$) are more suitable for the PVT bank. A simplified schematic of such a varactor is shown in figure 2.14.

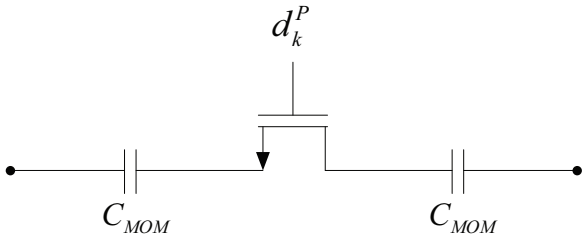

Figure 2.14: Small-signal model of a PVT bank varactor.

This varactor consists of two capacitors and a switch. Capacitors used in this design are rotated metal-oxide-metal (RTMOM) capacitors. Capacitance density over area, reliability, and availability of higher metal layers in these capacitors make them suitable for this design. NMOS transistors are used as switches in these varactors. The control bit is applied to the gate of the transistor. The control bit can set the varactor either in OFF state or ON state.

- When the control bit is high, the gate voltage is high. The transistor is then ON and conducting. Total capacitance of the varactor in this mode equals the series connection of the RTMOM capacitors.
- When the control bit is low, the gate voltage is low. The transistor is OFF and not conducting. Total capacitance of the varactor in this mode depends on the parasitics of the components.

These two states of the varactor will be discussed in detail. From now on the PVT bank varactors will be referred to as PB varactor for short.

PB varactor in ON state

When the control bit is high, the gate voltage of the NMOS transistor is at *Vdd* and the transistor is on and conducting. Equation 2.21 shows how the on-resistance of the NMOS is dependent on the transistor parameters:

$$R_{on} = \frac{1}{K\frac{W}{L}(V_{GS} - V_T)} \tag{2.21}$$

These parameters are

- $\frac{W}{L}$: wider transistors with shorter channel lengths can deliver less R_{on}
- V_{GS}: by increasing the gate-source voltage and therefore increasing the overdrive voltage, R_{on} decreases.
- V_T: lower threshold voltage will provide higher overdrive voltage and less R_{on}.
- K: This parameter is solely dependent on the technology.

The most important effect of R_{on} is the varactor loss. This effect can be examined using the quality factor introduced in chapter 1. In the ON state, the simplified small-signal model of the varactor can be seen in figure 2.15.

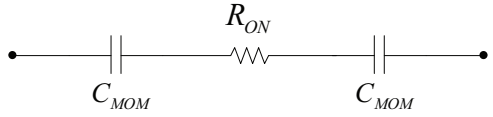

Figure 2.15: PVT bank varactor small signal model in ON state.

According to equation 2.3, the quality factor of this varactor in the ON state can be expressed as in equation 2.22:

$$Q_{on} = \frac{1}{R_{on}C_{on}\omega} \tag{2.22}$$

where $C_{on} = \frac{C_{MOM}}{2}$ is the varactor capacitance in the ON state and $\omega = 2\pi f$ is the angular frequency.

Conventionally, the loss in the inductor is the main source of power loss in the tank. This means that at low frequencies, the Q of the tank can be approximated by the Q of the inductor. Due to high frequency performance of the DCO and also the restrictions imposed on PB varactors by the tuning range specification, PB varactors loss is a considerable part

of the total tank loss in this design. So it is important to investigate different parameters that affect PVT bank quality factor.

In equation 2.22 It has been assumed that the quality factor of the RTMOM capacitors used in these varactors is infinity. This assumption is not true and RTMOM capacitors also have finite quality factor. Due to longer metal fingers in MOM capacitors which introduce more resistivity, larger capacitors have lower quality factor. The finite quality factor of the RTMOM capacitors becomes even more important in PVT bank since large capacitors are used (especially for the more significant varactors) for generating larger ΔC. However, due to tuning range restrictions on the PB varactors, it will be shown that switching transistors cannot be as wide as possible. This will introduce a comparatively large on-resistance which will limit the quality factor to an extent where the finite quality of the RTMOM capacitors becomes unimportant.

There are two ways to reduce the on-resistance of the NMOS:

- increasing the width of the transistor
- increasing the gate-source voltage of the transistor

Increasing the width of the transistor will result in better ON-state Q. However, by enlarging the transistor, parasitic capacitors at the source and drain terminals of the transistor also increase. As discussed in 2.5.3, these parasitic capacitors form most of the parasitics of the varactor in off-state. Since the on-state capacitance is limited by the series connection of the RTMOM capacitors, ΔC of the varactor decreases according to 2.6. This will directly affect the tuning range of the DCO. Tuning range specifications therefore define an upper limit on how large these NMOS transistors can be.

The other solution is to provide maximum gate-source voltage in order to minimize the on-resistance. Since the gate voltage is connected to Vdd, switch terminal voltage should be pulled down to the lowest power supply (which in this case is 0V). This biasing will provide enough overdrive voltage and also bring the transistor into deep triode. Two pull-down NMOS transistors are connected to the switch terminals to provide this biasing as shown in figure 2.16. The gate of these transistors can be connected to the control bit. When the control bit is high, these NMOS transistors turn on and pull down the transistor source and drain voltages to ground. These transistors are chosen to be as small (large channel length and short width) as possible so that the input impedance of these biasing paths is much higher than the on-resistance of the switching transistor.

RTMOM capacitors also contribute to the parasitics at the drain and source of the switching transistors. A simple model of a RTMOM capacitor is shown in figure 2.17 where C_p indicates the total parasitic capacitances to substrate and r_s is the series resistance. However, if the varactor switch is large enough and its on-resistance is low, these parasitics will

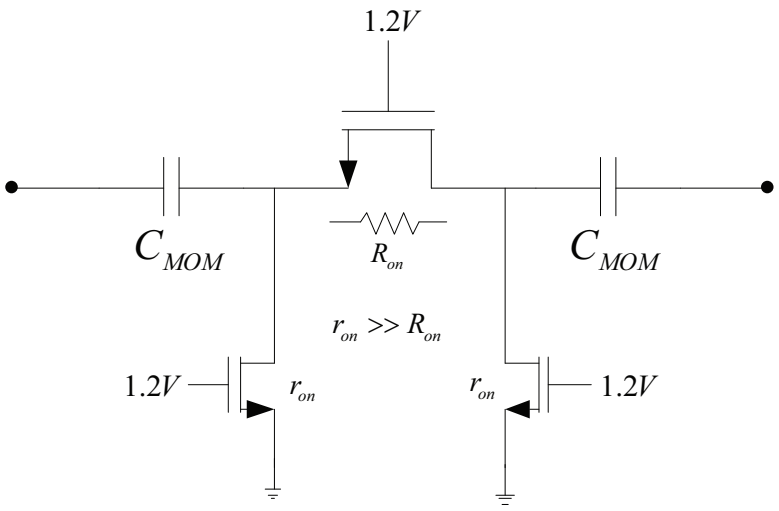

Figure 2.16: PB varactor switch biasing in the ON state.

not contribute to the total varactor capacitance in the ON state.

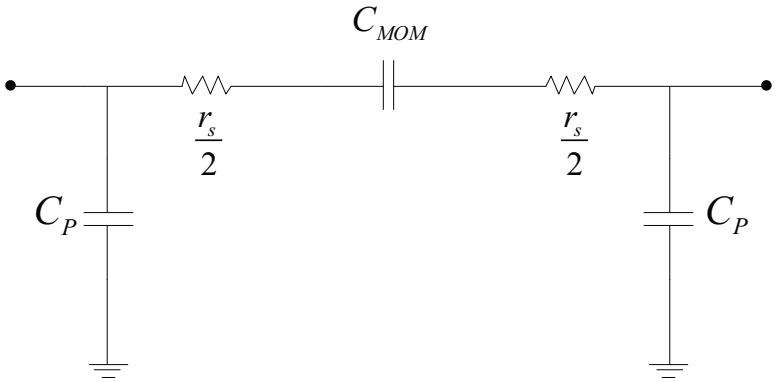

Figure 2.17: RTMOM capacitor model.

PB varactor in OFF state

When the control bit is low, the gate voltage of the varactor switch is zero, transistor is turned off and not conducting anymore. Before introducing a valid model for the varactor in the off-state, it is important to look at the varactor biasing once more. In the on-state two small NMOS transistors determine the DC level of the varactor switch terminals. When the control bit is zero in the off-state, these two transistors are also turned off and switch terminals are floating. In order to bias these nodes in the off-state, two PMOS transistors are added to the varactor as shown in figure 2.18 [20]. The two transistors also have to be

small (small gate width and large gate length) in order to create a high impedance signal path.

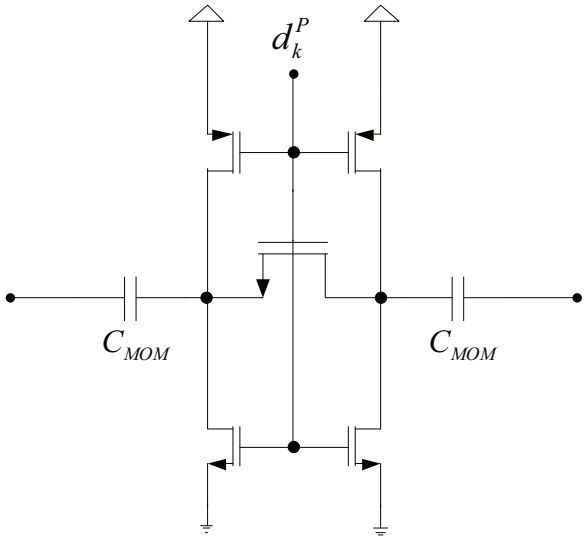

Figure 2.18: PB varactor switch biasing in the OFF state.

The impedance of the biasing path in the off-state (which is the on-resistance of the PMOS transistors) plays an important role in the performance of the varactor. In the ON state, this impedance is bypassed by the on-resistance of the switch which is much smaller than the on-resistance of the small biasing NMOS transistors. In order to find out the influence of the PMOS on-resistance on the varactor performance, a simple model for the varactor in the off-state is introduced in figure 2.19.

Node A and B in figure 2.19 are important to be investigated in detail since the off-state capacitance directly depends on the parasitic capacitances at these nodes. There are different components contributing to the total parasitic capacitance (C_P)at node A and B:

- Switch drain and source junction capacitors $(C_{db,sw})$: these capacitors form the main part of the parasitic capacitance at node A and B. Larger switches contain larger drain and source area which results in larger capacitance. So by reducing the size of the transistor, these parasitics can be reduced and larger ΔC is attainable. This is however in contrast with the requirements in the ON state where larger switching transistors are required to achieve enough quality factor. The layout of the NMOS transistor is symmetric so similar junction capacitances exist at source and drain nodes
- biasing transistors junction capacitors $(C_{db,bias})$: two NMOS transistors which provide desired DC level for the switch terminals in the ON state, are off now and their drain-bulk junction capacitor also contributes to the total parasitics at node A and B.

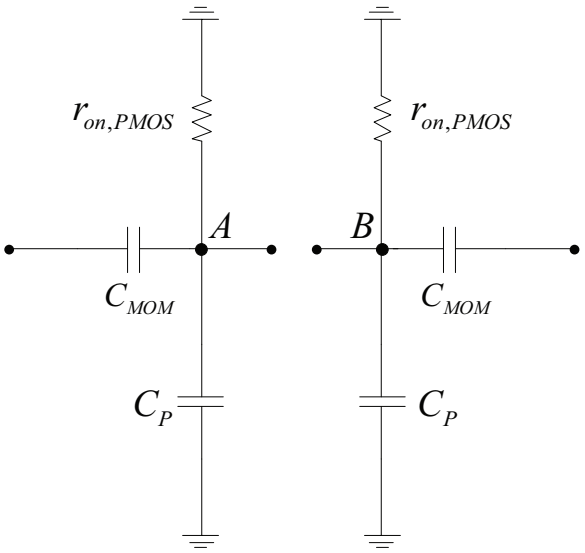

Figure 2.19: PB varactor small signal model in the OFF state.

Since these two capacitors are much smaller than the switch parasitics, this contribution is also small.

- RTMOM capacitor parasitics $(C_{p,MOM})$: a simple model for the RTMOM capacitors indicates that it also contains parasitics to the substrate. These parasitics can be simply modeled via two parasitic capacitors at each node to a third node which in this case is ground (as it will be shown in layout, MOM capacitors are placed in a local P-well). According to the placement of the varactor in the tank, one part of this capacitance will be placed at the output of the tank which acts as a fixed capacitance, and the other part is involved in the parasitics of node A and B (figure 2.17).

Equation 2.23 detemines the varactor capacitance in the off-state:

$$C_{off} = \frac{C_{MOM} + C_P}{2} = \frac{C_{MOM} + (C_{db,sw} + C_{p,MOM} + C_{db,bias})}{2} \tag{2.23}$$

where (C_P) is the total parasitic capacitance at node A or B.

There are a two important advantages in pulling up the voltage of the drain and source nodes while the gate voltage is low:

1. The drain-bulk diode will be reverse-biased which will result in minimum parasitics of the switch.

2. Due to certain signal swing at node A and B, there is a possible chance for latch-up. This will be prevented by assuring that the DC level voltages of these nodes are as high as possible.

Using these simple models for the varactor, the ON state and OFF state capacitances can be calculated as in equations 2.24 and 2.25 :

$$C_{on} = \frac{C_{MOM}}{2} \tag{2.24}$$

$$C_{off} = \frac{C_{MOM}C_P}{2(C_{MOM}+C_P)} \tag{2.25}$$

The capacitance step of the varactor can therefore be written as in equation 2.26

$$\Delta C = C_{on} - C_{off} = \frac{C_{MOM}^2}{2(C_{MOM}+C_P)} \tag{2.26}$$

It can be seen that in the ideal case, where there are no parasitics ($C_P = 0$), the OFF state capacitance is zero and $\Delta C = C_{on}$.

The quality factor of the varactor in the OFF state is determined by the finite quality factor of the RTMOM capacitors and the parallel connection of (C_P) and ($r_{on,PMOS}$). In order to find a better understanding on this, let's consider the small signal model in figure 2.20. Since the varactor is symmetric, it can be divided in two identical parts as shown in the figure.

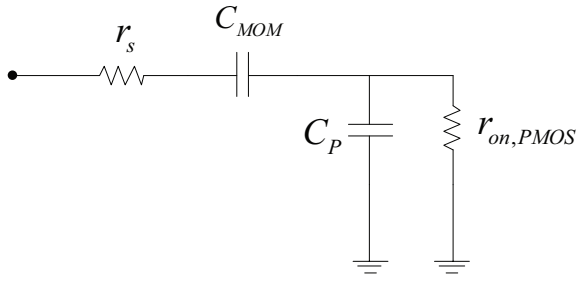

Figure 2.20: Simplified small signal model of a PB varactor in the OFF state.

Due to the finite Q of the RTMOM capacitor, a resistor (r_s) can be placed in series with C_{mom} to indicate the losses as shown in figure 2.20. Now the total quality factor of the varactor can be expressed as in equation 2.27:

$$\frac{1}{Q_{tot,off}} = (r_s + \frac{r_{on,PMOS}}{Q_P^2}) \times (\frac{C_{MOM}C_P}{C_{MOM}+C_P}) \times \omega \tag{2.27}$$

where $Q_P = r_{on,PMOS} \times C_P \times \omega$. This equation can be rewritten as in equation 2.28:

$$\frac{1}{Q_{tot,off}} = \frac{C_P}{C_P + C_{MOM}} \cdot \frac{1}{Q_{MOM}} + \frac{C_{MOM}}{C_P + C_{MOM}} \cdot \frac{1}{Q_P} \tag{2.28}$$

where $Q_{MOM} = (r_s C_{MOM} \omega)^{-1}$ is the quality factor of the RTMOM capacitor. So it can be seen that both quality factors of the RTMOM and parasitic capacitor are included with a certain factor. Since the parasitic capacitor is much smaller than the RTMOM capacitor, Q_{MOM} factor ($\frac{C_P}{C_P+C_{MOM}}$) in equation 2.28 is much smaller than Q_P factor ($\frac{C_{MOM}}{C_{MOM}+C_P}$). This indicates that Q_P contribution to $Q_{tot,off}$ is much more than Q_{MOM}. Another way to explain this equation is that the losses of the parasitics (through the on-resistance of the PMOS transistors) are the main source of loss when the varactor is in the OFF state.

In order to increase the varactor Q in the OFF state, the resistive biasing path must be increased. So far, the only resistivity is provided by the small PMOS transistor on-resistance. One way to increase the OFF state quality factor is to add a resistor (R_s) to the drain of the PMOS transistors as shown in figure 2.21.

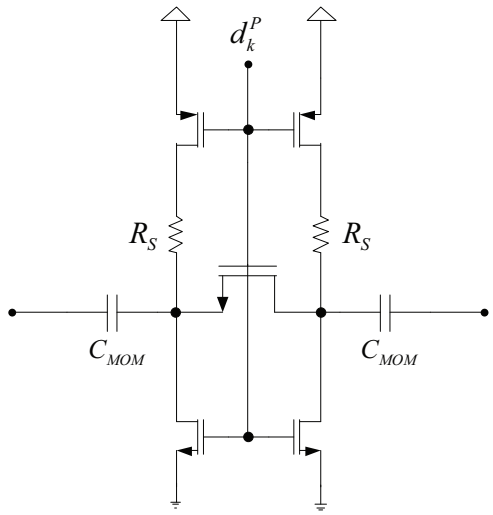

Figure 2.21: OFF-state Biasing path after adding series resistors.

In figure 2.22 the effect of R_s on the OFF state Q is shown. The ON-state Q does not change since it depends on the on-resistance of the switching transistor. It can be assumed that R_s can be increased as much as needed to achieve the desired quality factor. This large resistor is the main cause of DCO choking which will be described in detail in section 2.5.4.

Another way to increase Q_{off} is to use a component that provides high resistivity in its path so that Q_P is increased. This component could be a PMOS transistor in its subthreshold region as shown in figure 2.23. When the switch is on, pull-down NMOS transis-

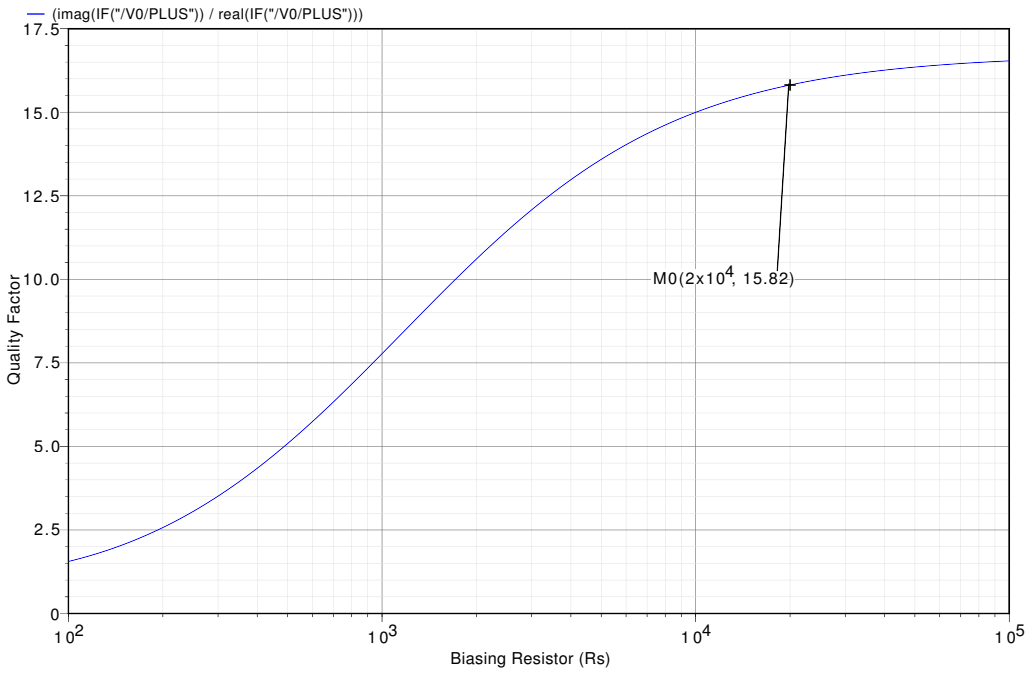

Figure 2.22: OFF state quality factor of the PB varactor as a function of biasing resistor.

tor provide much less resistivity so that drain and source voltages are pulled down. In the ON state, the sub-threshold conductivity of the PMOS transistors will eventually pull up the switch terminals to Vdd. This idea was abandoned due to high $1/f$ noise contribution of the PMOS transistors which is upconverted in the tank and effects the phase noise in -30 dBc/Hz region.

In order to decrease the parasitics, PB varactor can be re-arranged as in figure 2.24. Instead of two pull-down NMOS transistors and two pull-up PMOS transistors, a small inverter is used to control the biasing of the switch terminals via two resistors. This will reduce the parasitic effect of the biasing transistors and provide slightly larger ΔC for the varactor. The inverters are small and static so their power consumption is negligible.

In figure 2.25, the capacitance of the most significant PB varactor is plotted as a function of the width of the switch. It can be seen how the OFF-state capacitance is increased by the switch width in an almost linearly manner.

The quality factor of the most significant PB varactor is shown in figure 2.26.

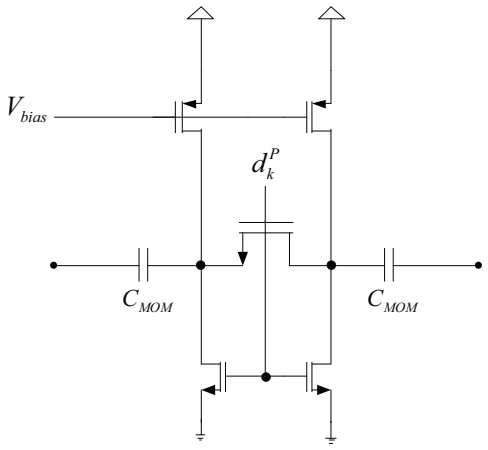

Figure 2.23: OFF-state biasing for PB varactors using PMOS transistors in weak inverstion.

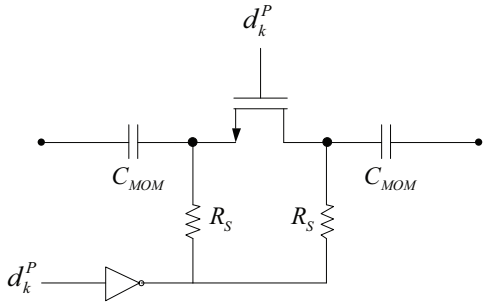

Figure 2.24: Final PB varactor configuration.

2.5.4 DCO Choking

One of the main problems during the design of the PVT bank is DCO choking. This problem occurs when a big capacitance jump is happening in PVT bank specially the most significant bits. Suppose all varactors of the PVT bank are switching from the ON state to the OFF state. Switching transistors gate voltages are being pulled up while their drain and source voltages are being pulled down. As it was mentioned in 2.5.3, R_S is chosen to be high enough to provide enough Q in the OFF state. However, this resistor and the parasitic capacitors at drain and source terminals provide a large time constant which makes the transition at switch terminals take longer time. The consequence of this long transition is that since these two nodes were previously pulled up to Vdd, even with the high voltage at the gate, V_{GS} is still very small at the time of switching and the switch conductivity is low. As the switch terminal voltages begin to drop, the switch gradually turns on. During this transition, DCO has to tolerate the low Q of the varactor with half-turned-on switches.

As mentioned before, PVT bank quality factor plays an important role in the Q of the tank. DCO cannot tolerate this temporary low Q and oscillation dies out. In figure 2.27 this

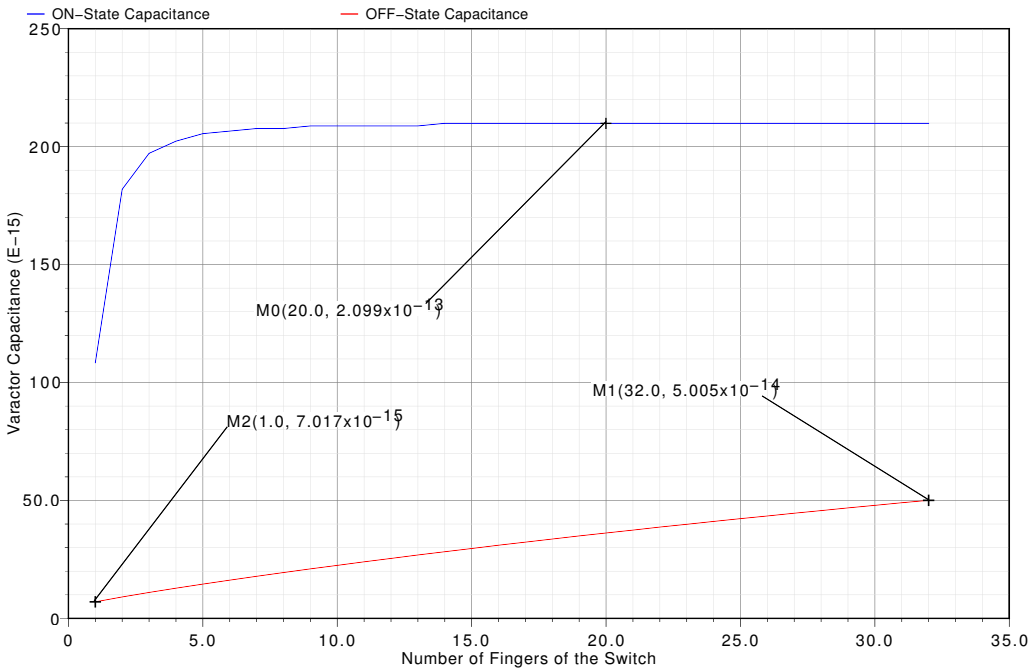

Figure 2.25: Capacitance of the most significant PB varactor for different number of fingers (W=2u, L=40n).

phenomenon is illustrated. A global control bit is used to turn on or off all the PB varactors at the same time. In this figure, the gate and the drain/source transient responses are also shown.

It can be seen that during the on-to-off transition, oscillation also starts to fade for a very short time but it recovers to full swing. This is again due to the fact that gate voltage does not change instantly and there is a short transition time especially for the most significant varactors which have larger switches. The problem with the long transition time of drain and source still exist but will not have an effect on the state of the switch since the high voltage of the gate guarantees that the switch is off. Any minor effect beside choking will fade away after the transition, but oscillation does not stop.

In order to have a better understanding of exactly what happens to the varactor Q during the off-to-on transition, figure 2.28 shows the Q of the most significant varactor versus the gate-source voltage of the switching transistor. It can be seen that Q has a minimum value for a values of V_{GS} around the threshold voltage.

In order to solve this problem, the PVT varactors are provided with two control signals

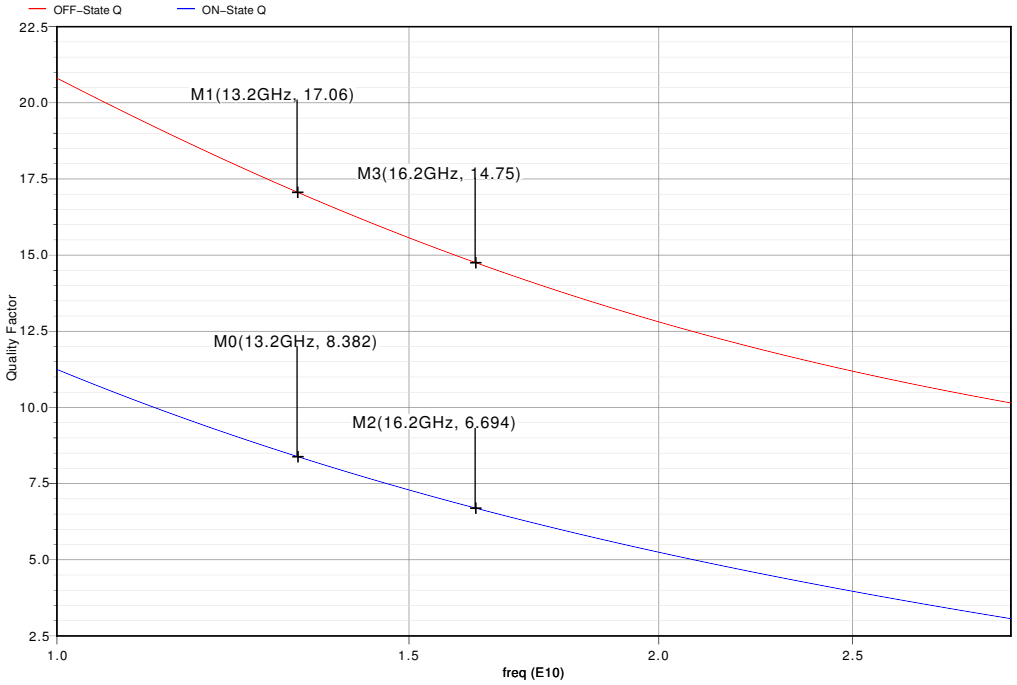

Figure 2.26: Quality factor of the most significant PB varactor in ON and OFF states.

instead of one: one signal controlling the gate of the switch (b_G) and the other one controlling the drain/source voltage (b_{DS}). b_G is applied directly to the switch whereas b_{DS} is applied to the biasing inverter as shown in figure 2.29. These two bits statically have the same value. The only difference between the two is when they are changing from zero to one.

As it is shown in figure 2.30, b_{DS} becomes one a certain time before b_G does. This will assure that the drain and source voltages of the switch are pulled down to zero before the gate voltage becomes high and the switch turns on. This way, the gradual increase of the V_{GS} and the low quality factor in this transition is avoided. It can be seen in figure 2.30 that choking does not happen anymore when all the PVT varactors change go through the off-to-on transition.

The time difference indicated in figure 2.30 can be provided by the reference clock of the ADPLL. The reference clock period is 24ns which is enough for the drain/source to settle. So b_{DS} will become high one reference clock cycle before b_G becomes one. It is important to mention that the actual frequency change in DCO happens when b_G becomes one since that is when the switch is officially turned-on.

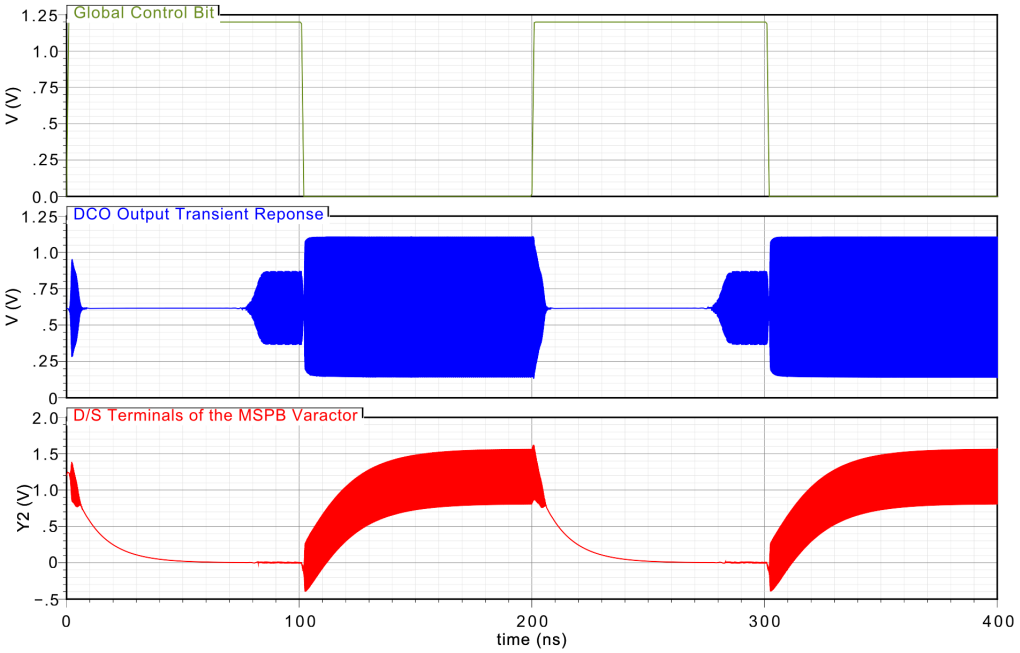

Figure 2.27: DCO choking: The oscillation stops when the global bit goes from 0 to 1.

So far, It was assumed that the on-to-off transition is the same as before. It means that no time interval between b_{DS} and b_G are needed for this transition. But an important issue arises when some particular transitions are happening. This will be described by an example:

As it was mentioned before, PVT varactors are binary weighted . According to section 2.5.2, PVT bank consists of seven bianary varactors. these varactors are controlled by two seven bit control words for the drain/source and the gate. The control word range is from $(2^0 = 0)$ to $(2^7 = 127)$.Assume the 63-to-64 transition where all the varactor are going to the off-state except for the most significant varactor which is changing to the on-state. If this transition is supposed to happen at time t_0, the most significant b_{DS} must change state one reference clock cycle before t_0 so that the states of the varactor change all at the same time. Otherwise, for one reference clock cycle all varactors will be in off-state until the most significant varactor gate voltage becomes high. This frequency jump will corrupt the functionality of the ADPLL. So it is important to synchronize the gate control bits because they are the real indicators of the change in the varactor states.

There are other ways to solve the choking problem which mostly require additional components [1]. These solutions are not preferred in order to avoid extra parasitics and tuning range limitation.

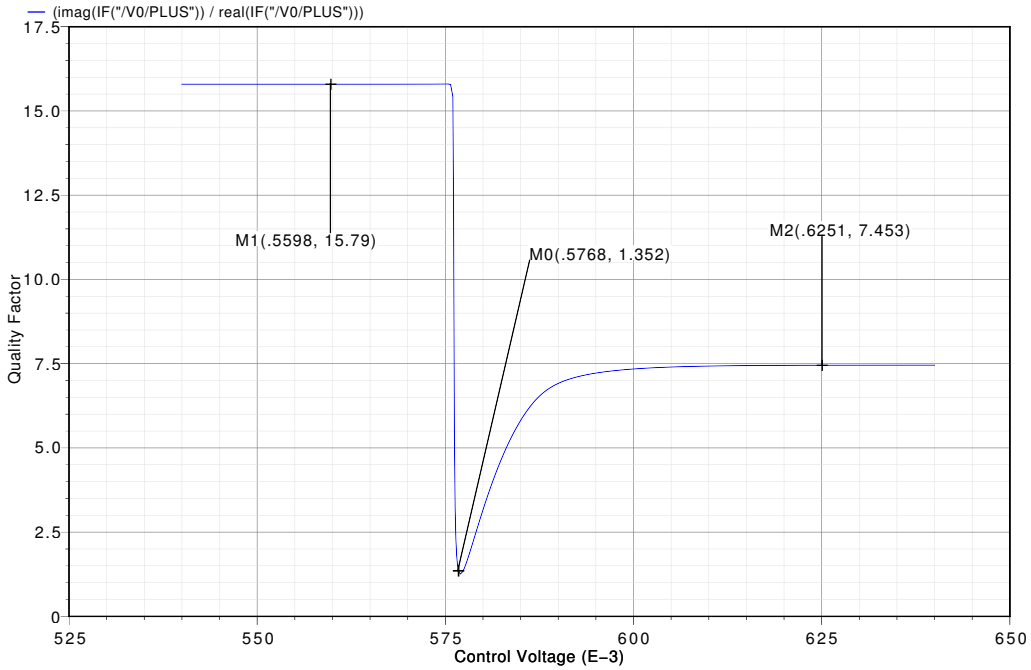

Figure 2.28: Quality factor of the most significant bit as a function of the control voltage

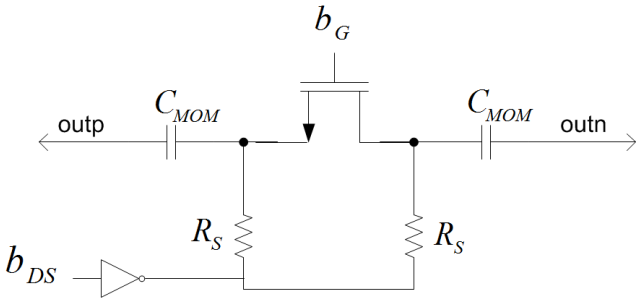

Figure 2.29: Final version of the PB varactor: gate and D/S control signals are seperated.

2.5.5 Acquisition Bank

The varactor in the acquisition bank are the same as the PVT varactors. There are six binary-weighted varactors. The most significant ΔC of this bank is four times the least significant ΔC of the PVT bank as described in 2.5.2. AB varactors do not have the same issues as the PB varactor for two reasons:

1. Since the RTMOM capacitors are smaller than PB varactors, smaller switches can

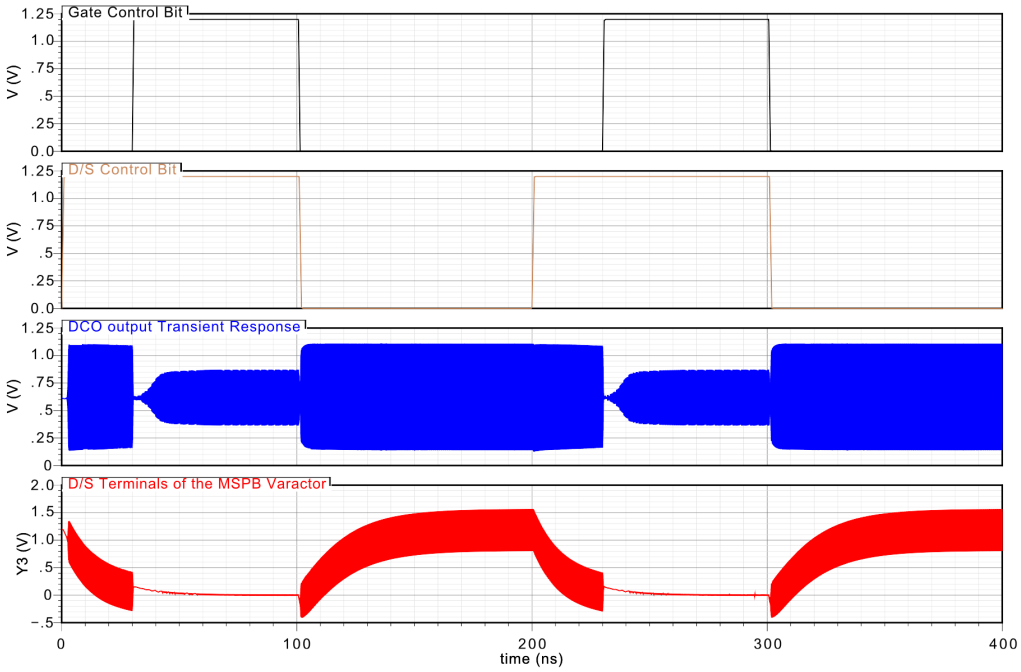

Figure 2.30: DCO transient response for when the gate and D/S control bits are seperated.

provide enough quality factor in the off-state, which will result in smaller parasitics and therefore higher quality factor in the off-state.

2. Total capacitance contribution of the acquisition varactors to the tank is much less than the PB varactors. Therefore, even if they have poor quality factor, they are only a small part of tank capacitance which will not let the DCO suffer.

An AB varactor is shown in figure 2.31. It can be seen that despite the PB varactors, only one control bit is enough to determine the state of the varactor. This is due to the fact that according to the two reasons discussed previously, AB varactor state changes even in the worst case will not cause choking. On the other hand, transient time of the state changes are small and acceptable by ADPLL requirements.

The capacitor of the varactor is a function of the width of the switching transistor. This is shown in figure 2.32.

The quality factor of the most significant acquisition bank varactor is shown in figure 2.33 both in off-state and on-state.

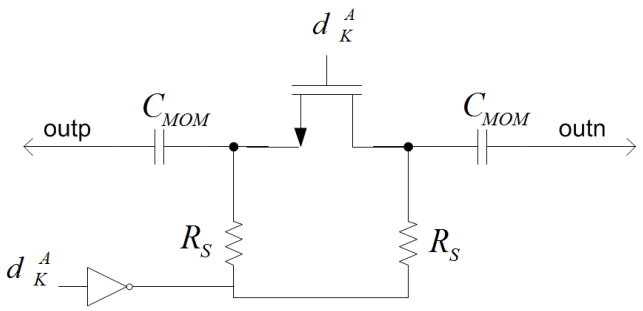

Figure 2.31: Final schematic of the AB varactor.

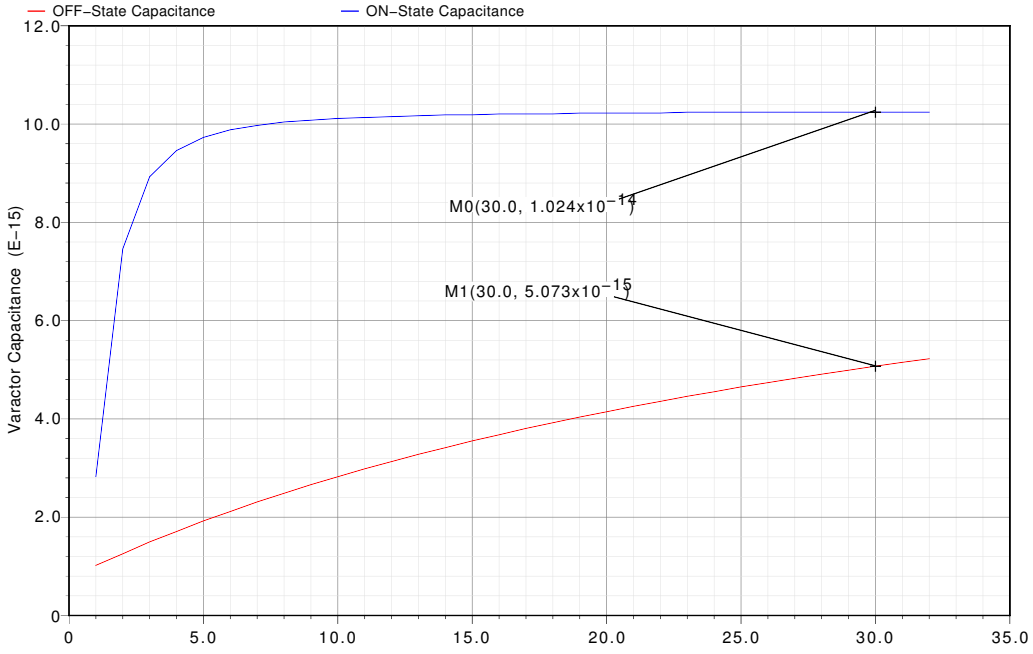

Figure 2.32: Capacitance of the most significant AB varactor as a function of the switch width (W=600n, L=40n).

Linearity of the acquisition bank is as it was for the PVT bank. The requirement is again one LSB ΔC.

2.5.6 Tracking Bank

Tracking bank main purpose is to provide high frequency resolution over a specified frequency range that acquisition mode has landed on. TB varactors are design in such a way

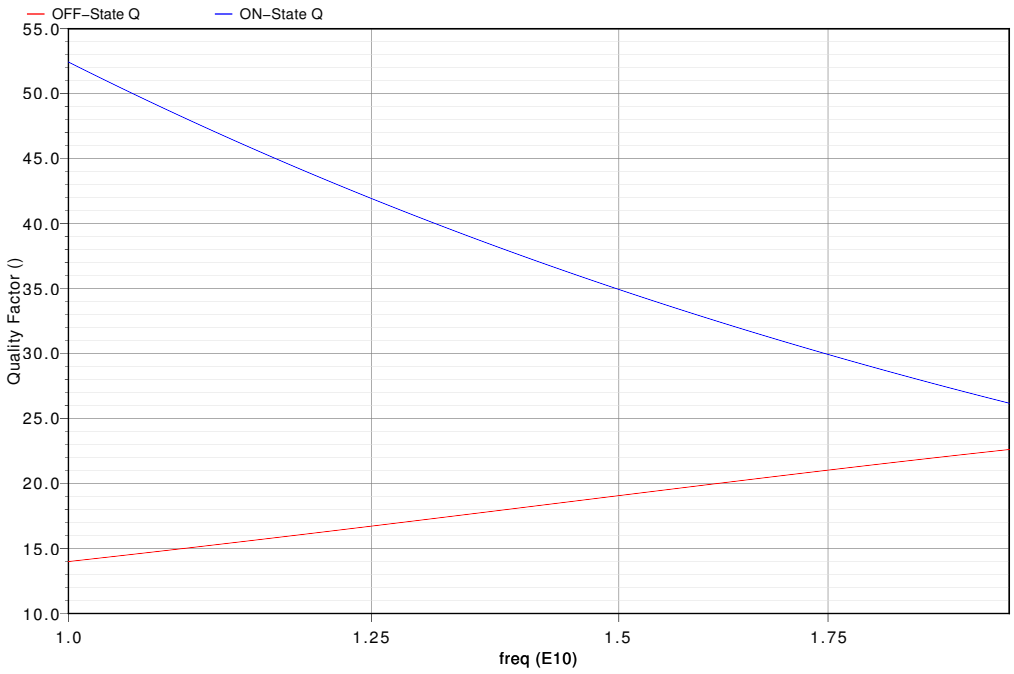

Figure 2.33: Quality factor of the most significant AB varactor in ON and OFF state.

that they provide small ΔC. The required ΔC is determined according to the value of the inductor and the frequency of operation. As it was discussed in section 2.5.2, starting off with an estimation of the inductor value, ΔC of the TB varactors can be determined using equation 2.15. Using equation 2.1 this equation can be rewritten as in equation 2.29.

$$df = (4\pi^2 f^3 L)dc \tag{2.29}$$

According to this equation, it can be seen that the frequency step of the TB varactors is maximum at high frequencies. Using the frequency resolution specification (240KHz), the initial estimation of the inductor (300 pH) and the highest frequency of the DCO, ΔC_{TB} can be determined. Simulations show a larger ΔT_{TB} for slow process corners. So after considering a certain headroom for possible increases of ΔC_{TB}, this value is set to 10aF.

According to section 2.5.2 total frequency range of tracking bank should be 4 times the frequency step of the acquisition bank. Since ΔC_{PB} is 160aF, $\Delta C_{tot,TB}$ should be 640aF. The small value of ΔC_{TB} will not be possible to achieve with PB and AB varactors. In order to have a more reliable design, a new varactor is introduced figure 2.34.

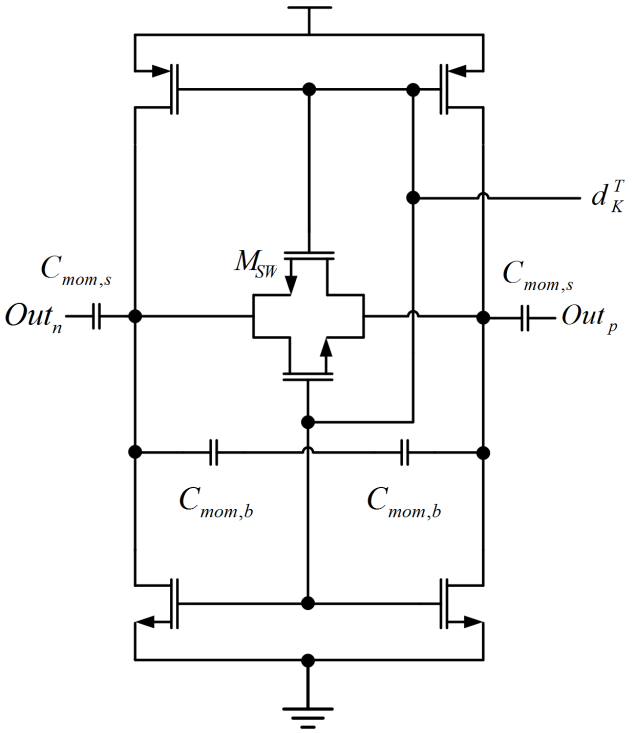

Figure 2.34: Schematic of the tracking bank varactor: the weak biasing PMOS and NMOS transistors to determine the DC voltage of the switch terminals.

The idea is to use two small RTMOM capacitors $(C_{mom,s})$ and two large ones $(C_{mom,b})$. When the switch is on, the two big capacitors are shorted by a switch and they do not contribute to the varactor capacitance. The on-state capacitor is therefore determined by the series connection of two $(C_{mom,s})$. This is shown in equation 2.30:

$$C_{on}^T = C_{mom,b}/2 \tag{2.30}$$

When the switch is off, $C_{mom,b}$ capacitors get in series with $C_{mom,s}$ capacitors and the total capacitor is then defined as in equation 2.31:

$$C_{off}^T = (C_{mom,s} + C_{mom,b})/2 \tag{2.31}$$

Using these two equation, capacitance step of the tracking bank can be calculated as in equation 2.32

$$\Delta C = C_{on} - Coff = \frac{1}{2}\frac{C_{mom,s}^2}{C_{mom,s} + C_{mom,b}} \tag{2.32}$$

Since $C_{mom,b}$ is much larger than $C_{mom,s}$, very small capacitance step is attainable with this varactor. In order to minimize ΔC_{mom}^T, $C_{mom,s}$ should be minimized and large $C_{mom,b}$ values should be chosen. In order to do so, smallest RTMOM capacitor was chosen for

$C_{mom,s}$.

Biasing of the switch drain/source nodes are done like that of the PB and AB bank. Instead of one inverter and two resistors, two small inverters are placed at the switch terminals to determine the DC level of these nodes. parasitics at these node are not important since $C_{mom,b}$ is much bigger than the parasitics of the inverters.

In figure 2.35, the capacitance of the TB varactor is shown as a function of the control bit voltage.

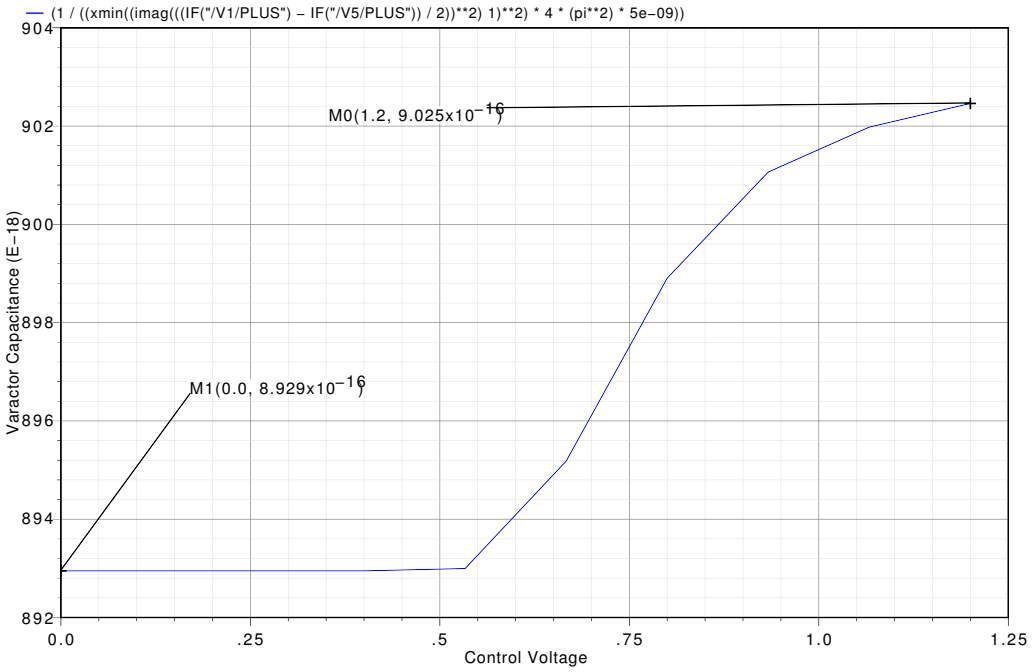

Figure 2.35: Quality factor of the TB varactor as a function of the control bit voltage.

In figure 2.36, the high quality factor of the TB varactor is shown. It can be seen that the quality factor of this varactor is much larger than that of the PB varactors. Post-layout simulations will show that due to the large area of the tracking bank, total quality factor of the tracking bank is degraded considerably due to long routing (see chapter 3).

The most important characteristic of the tracking bank is linearity. There are 64 varactors which need to provide capacitance step of ΔC_T. In order to find out the mismatch error specification for these varactors, first the fractional part of the tracking bank is introduced.

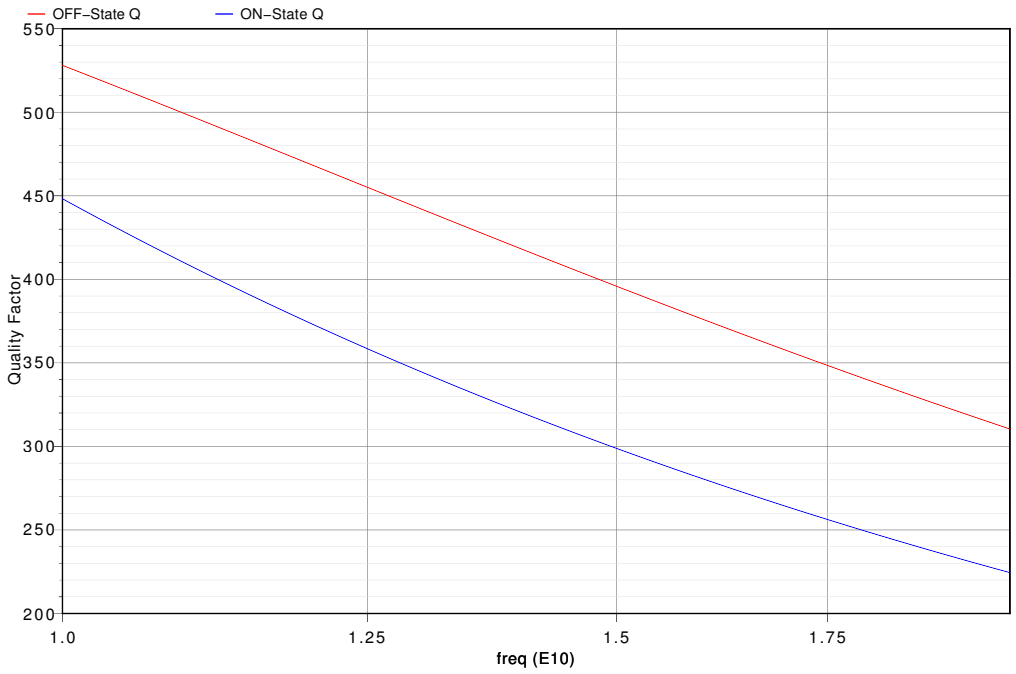

Figure 2.36: Quality factor of the TB varactor in ON and OFF states.

Fractional part of the tracking bank will provide the DCO with higher frequency resolution. The idea is to use high-speed dithering of the control bit. The high-speed dithering of the control bit will generate a stream of 0's and 1's the average of which approaches low frequency fractional input. The frequency of dithering in this design is set to the be $1/8$ of the oscillator clock frequency ($f_{dith} = 500MHz$).

The output of the high-speed dithering is applied to the gate of one TB varactor as its control bit. This dithering signal is provides by a 1st order sigma-delta modulator with 5 bit fractional input. 5-bit fractional input corresponds to a frequency resolution of $\frac{1}{2^5 \Delta f_T = \frac{1}{32} 240KHz = 1.6KHz}$. Assume the input of the sigma-delta modulator is n. This means that n one's and $32-n$ zeros are applied to the fractional varactor. During one reference clock cycle, this high-speed dithering happens numerous time so that the average capacitance value of the varactor can be expressed as in equation 2.33:

$$C_{FT} = \frac{n \times C_{on,T} + (32-n) \times C_{off,T}}{32} \tag{2.33}$$

The average capacitance step in this case can also be expressed as in equation 2.34

$$\Delta C_{FT} = \frac{n}{32} \Delta C_T \tag{2.34}$$

Chapter 3

Frequency Dividers

3.1 Introduction

According to the frequency planning mentioned in 2.2, DCO frequency range is such that the low-band and high-band frequencies are covered by frequency dividing blocks which follow the DCO as shown in figure 3.1. As calculated before, the original frequency range requirement for the DCO is 13.2 $GHz - 16.2\ GHz$. The high tuning range of the DCO is covered using switched-capacitor varactors. Due to the change in characteristics of the varactors when they are switched from one state to the other, DCO output characteristics also varies through the frequency range.

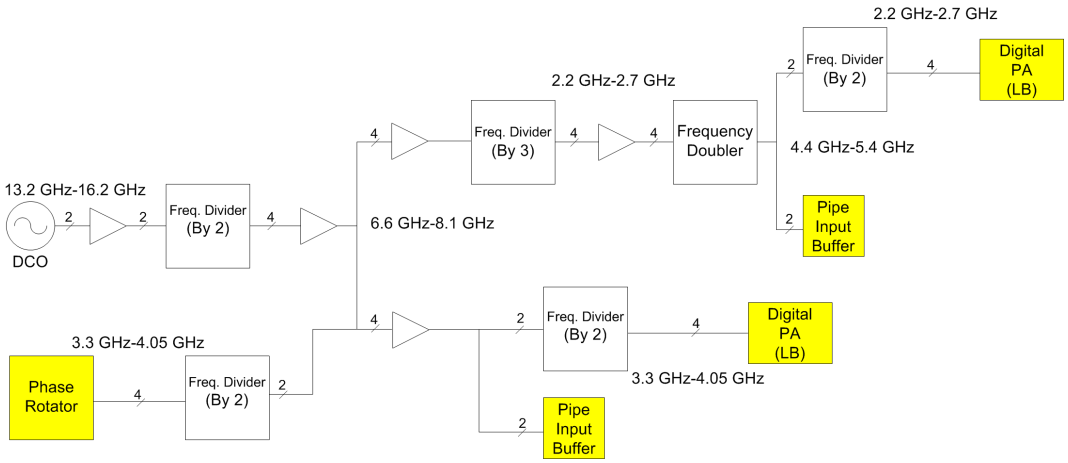

Figure 3.1: DCO system architecture as discussed in 2.2.

The main variation is DCO output voltage swing. As described in chapter 2.5, since PVT varactor switches are chosen to be as small as possible in order to reduce parasitics and increasing the tuning range, their on-resistance in the ON state imposes a relatively large resistive path and limits the output swing. This is the main drawback of a low-power

DCO with high tuning range.

The high frequency output of the DCO has to be delivered to the first dividing block: divide-by-2 frequency divider. Two important factors determine the interface between the DCO outputs and the frequency divider:

1. Frequency divider input requirements roughly determine the divider input voltage swing needed for the divider to operate at high frequencies and generate outputs with certain noise specifications.
2. Input capacitive load of low-noise frequency dividers is usually large. This means that direct connection of the two introduces a large capacitor to the tank and tuning range decreases.

For a low-noise low-power oscillator, inverters are a good choice to be used as buffers. Moderate-sized inverters can operate at high frequencies and add little noise to the signals. The main drawback of using only inverters in this design case is the low gain due to the high-frequency operation and the considerable capacitive load of the divider. As shown in figure 3.2, at such high frequencies inverters cannot produce a reasonable gain. So they do not seem to be a good choice to be used as DCO output buffers.

On the other hand, as it will be mentioned in 3.2, a CML-based divider is used as the first divide-by-two frequency divider. This divider does not need a high-swing input for its operation (although certain requirements are mentioned later in 3.2 in order to generate low noise floor at the output). So the main purpose of the buffer is to deliver the high-frequency low-swing outputs of the DCO to the divider without loading the LC bank.

In this design case, two cascaded inverters are used as the DCO output buffer. The first inverter which is connected directly to the DCO is moderately sized. Large inverters will load the tank and will not do much signal amplification due to the high frequency signals. On the other hand it has to be large enough so that the inverter noise floor is not considerable. The second inverter is larger to be able to drive the input capacitance of the divide-by-two frequency divider.

There are two ways to connect the first inverter to the DCO :

1. DC coupling: DCO outputs are directly connected to the inverters input. Input DC level of the inverter is then determined by the DCO output DC level.
2. AC coupling: a relatively huge capacitor is placed between the DCO and the inverter which only allows the high-frequency signals to pass through and isolates the DC levels. In this case, a biasing scheme is needed to determine the DC level at the input of the inverter.

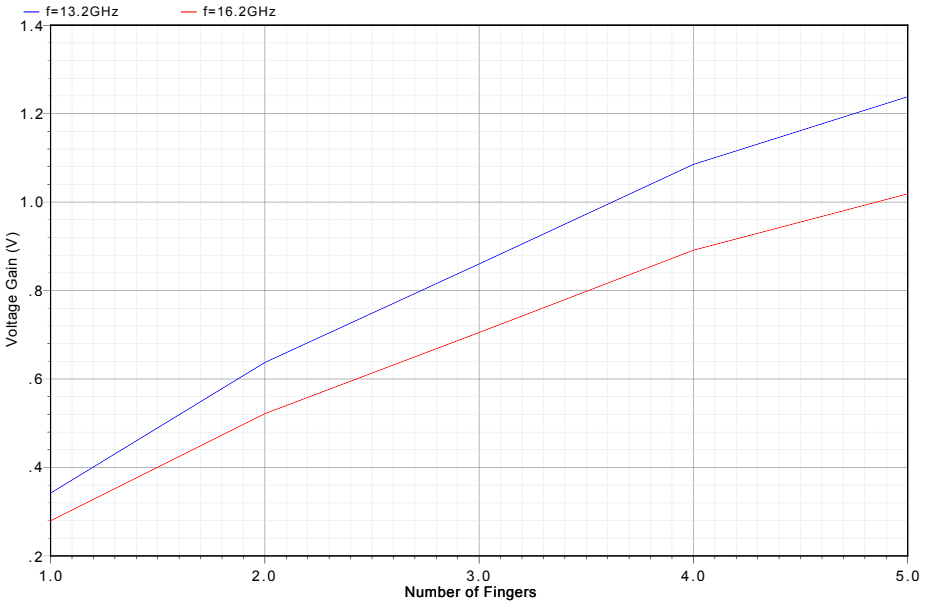

Figure 3.2: AC simulation shows the small-signal voltage gain of an inverter for different inverter sizes. The load is constant for each simulation and is an inverter with $W_p/W_n = 6u/3u$.

These two different schematics are shown in shown in figure 3.3.

Due to the DC level variation of the DCO output which can be due to process, temperature or voltage variations, the DCO output voltage has to be carefully examined in different corners in order to make sure that the inverter is not driven out of its linear region. The advantage of DC coupling, on the other hand, is avoiding the use of noisy passive elements for the inverter biasing and also the parasitics of the AC-coupling capacitor.

AC coupling makes sure that the inverter is biased at its linear region regardless of the DCO. There are different ways to bias the input node of the inverter:

- Using passive elements: a large resistor can be placed between the input and the output of the inverter as shown in figure 3.4. This resistor has much larger impedance than the input capacitance of the inverter so that the actual path of the signal is through the gates of the transistors and not through the resistor. On DC level, this resistor makes sure that the input and the output of the inverter have the same DC voltage which brings the inverter in the middle of the linear region and guarantees maximum voltage gain. By choosing a minimum value for the biasing resistor so that there is

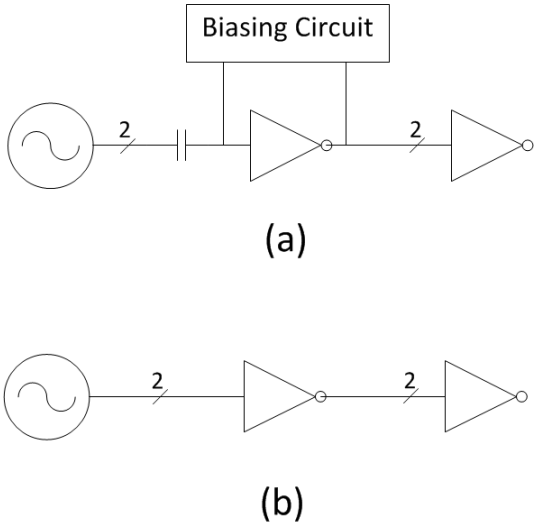

Figure 3.3: Two different connection between the DCO core and the inverter (a) AC coupling (b) DC coupling.

no significant gain loss in the inverter, the effect of the resistor thermal noise on the inverter's output noise floor can be minimized.

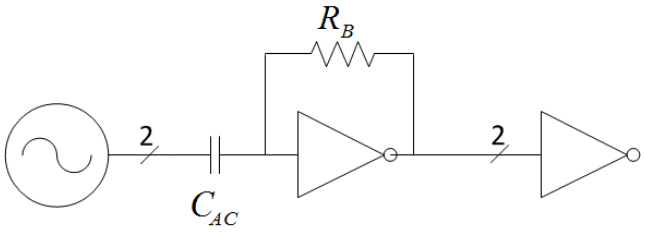

Figure 3.4: AC coupling using a large capacitor and a biasing resistor.

- Using a small-sized replica: Another way to bias the inverter is to use a minimum-sized replica of the inverter which has the same ratios as the original one. The output and input of this inverter is shorted and connected to the input of the original inverter. This biasing circuit is shown in figure 3.5.

  There are two reasons why this replica has to be minimum-sized: minimizing power consumption and providing a high-impedance path for the signal in the biasing network. The drawback of this schematic is that due to the small size of the replica, mismatch errors can be relatively big and the biasing voltage variation can bring the original inverter out of the linear region. This schematic is not self-correcting and this degrades the performance of the inverter.

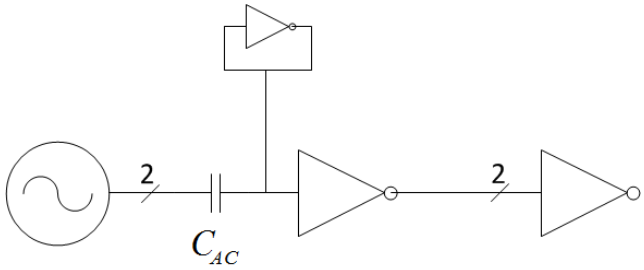

Figure 3.5: AC coupling using a small replica of the original inverter with shorted input/output.

3.1.1 Phase noise degradation in the $1/f^3$ region

By adding an inverter to the outputs of the DCO, the input capacitance of the inverter is added to the total capacitor of the LC tank and the maximum DCO frequency is decreased. The inverter input capacitance is mainly the gate capacitances of the NMOS and the PMOS of the transistors. As shown in figure 3.6, by adding the inverter, the phase noise is increased in the $1/f^3$ region.

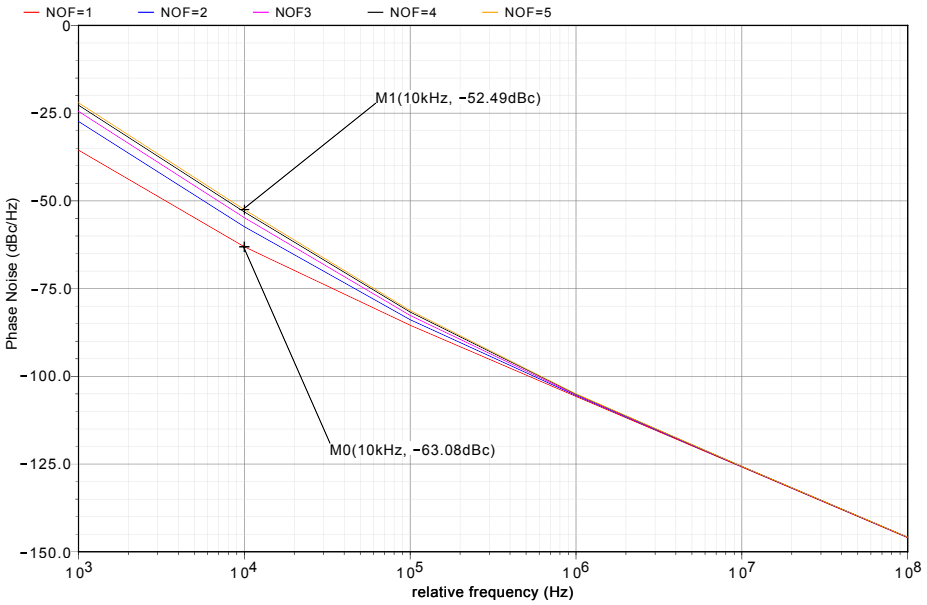

Figure 3.6: Phase noise degradation for different output inverter sizes

In order to find out the reason for this phase noise degradation, in figure 3.7 the input

capacitance of the inverter is plotted versus the input voltage of the inverter. It can be seen that the input capacitance is changing as a function of the input voltage. This change is the source of modulation of any inverter noise which exists at the input, which in this case is the 1/f noise of the transistors. It can be concluded that larger inverter contribute more noise to this mechanism and therefore phase degradation is worse as shown in figure 3.6.

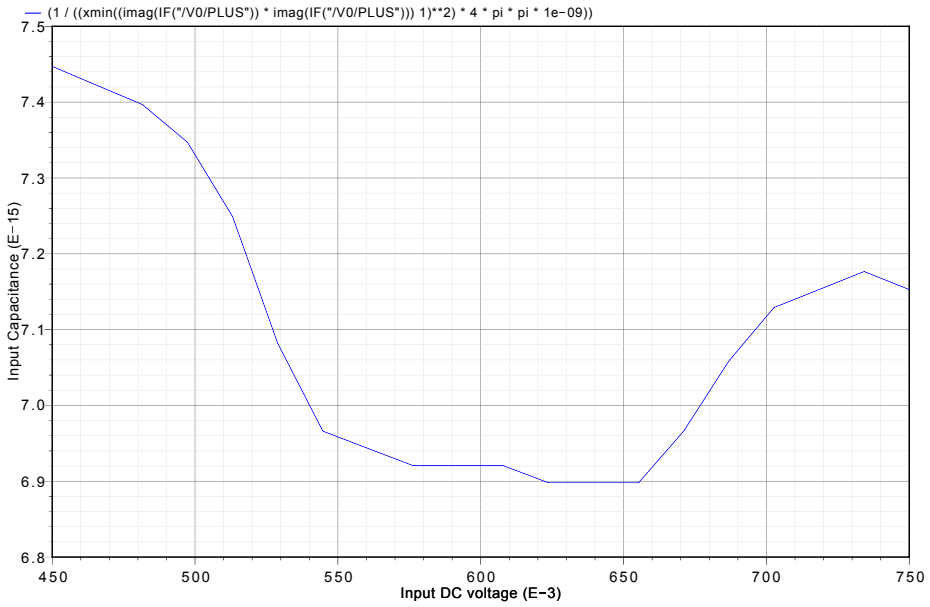

Figure 3.7: Inverter input capacitance as a function of the input voltage

Another observation shows that for the DCO outputs with lower swing, phase noise degradation is smaller. This can be also explained using figure 3.7 where lower input voltage swing results in lower change in the input capacitance.

Since large inverters are needed to generate less noise and drive the next stage inverters, a medium-sized inverter is chosen as the first buffering stage to compensate for two purposes: minimizing DCO phase noise degradation in the $1/f^3$ region and noise floor at the output of the buffers. The second inverter is chosen to be larger to be able to drive the divide-by-2 frequency divider with enough amplitude.

3.2 CML-Based Divide-by-2 Frequency Divider

The first dividing block is a divide-by-two frequency divider as shown in figure 3.1. The high frequency and the low swing of the inputs of this divider make this design a bit chal-

lenging. For achieving low phase noise with minimum power consumption, dynamic frequency dividers seem to be a proper choice for this design. Dynamic Dividers internal node voltage swings are high and the output states are stored in the parasitics of the divider instead of internal latches or any other memory components.

Despite of its advantages, this divider has lower maximum operating frequency compared to CML (current mode logic) dividers. This is due to the large swing of the internal nodes. If the rising and falling times of the full-swing internal voltages are comparable to the input signal period in high frequency operation, at some point the divider fails to follow its inputs and the frequency division ratio changes. This will determine the maximum operating frequency of the dynamic divider. Although dynamic dividers are not used in the first dividing block, they are used later at the end of the dividing chain where the frequency is much lower and dynamic dividers are a better choice as low-power low-noise frequency dividers.

The most important advantage of CML-based dividers is the ability to operate at much higher frequencies compared to the dynamic dividers [2], [9], [15]. CML-based dividers can be designed in such a way that make them capable of operating with very low-swing inputs around the optimal frequencies. This important characteristic makes it a suitable choice for the first dividing block.

The initial CML-based divide-by-two frequency divider used in this design is shown in figure 3.8. The whole divider is a D flip-flop realized using CML blocks, with feedback applied from its differential outputs back to its inputs [17].

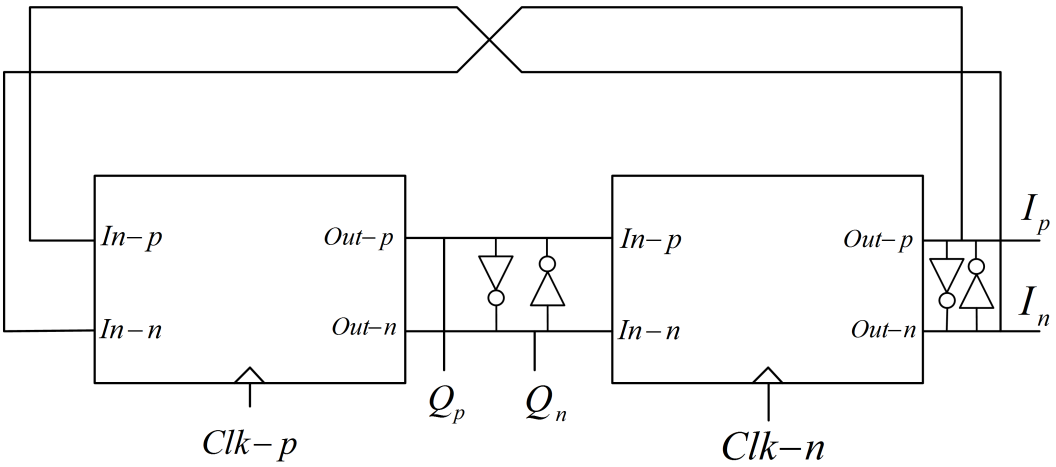

Figure 3.8: Schematic of the frequency divider containing two CML latches [17].

Differential outputs of each CML block can be realized as the differential in-phase and quadrature-phase outputs of the divider. Although it is convenient to analyze a clock divider

based on standard digital circuit behavior, in reality such circuits used in high frequencies behave more like complex dynamic systems [19]. This usually happens when the frequency approaches the time constant at the output of the divider.

A CML latch is shown in figure 3.9.

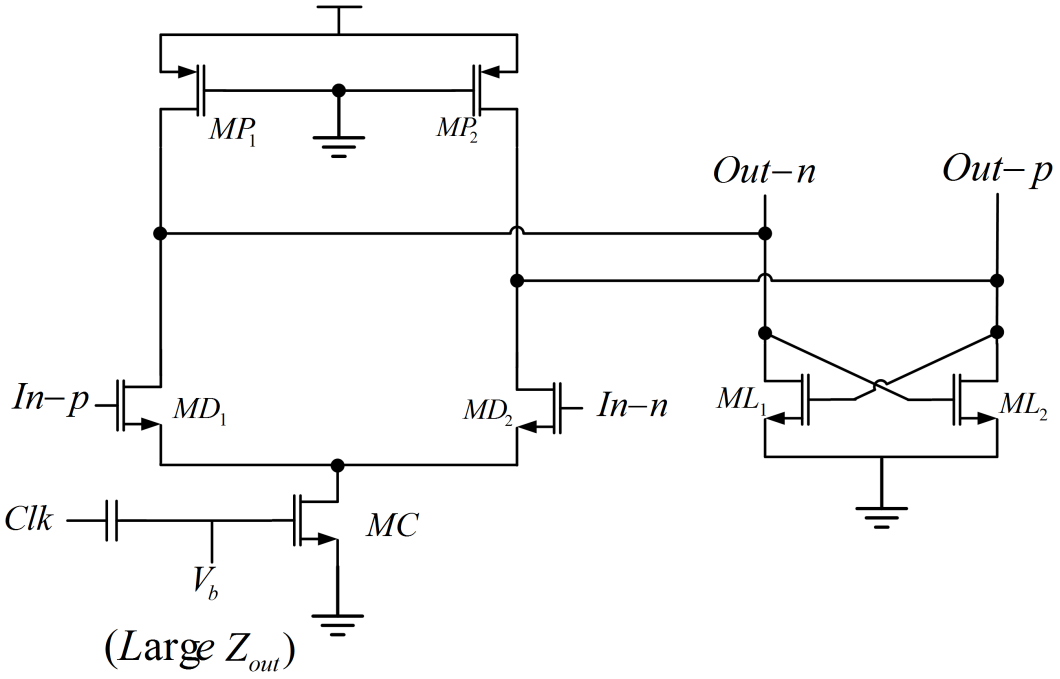

Figure 3.9: Schematic of a CML latch used in the frequency divider of figure 3.8.

The most important difference with conventional latches as in [19], is that the current source at the source of MC is removed. This is done for operation with lower supply voltages as in this case. This means that the current of the latch does not depend on a tail current source anymore [17]. In this case, the clock transistor MC, experiences class-AB switching. Class-AB switching would float more current at the peak of the input and improve the speed of the latch [17].

Another difference with conventional latches is the use of PMOS transistors MP, instead of load resistors [3]. The gate of these transistors is connected to ground so that they function as variable resistor whose value is dependent on drain-source voltage across the transistors. This is helpful when the output is being pulled up to Vdd: when the output voltage is increasing, drain-source voltage of the MP transistor decreases and the on-resistance becomes smaller, making the output transition faster. The area of the PMOS transistors is also much smaller than that of resistors. This is also helpful for reducing interconnects in the divider's layout.

MC transistor is driven by the input clock signal. As MC is made smaller, a bigger differential input is required to switch them [18]. This transistor is conducting in half of the differential input clock period. MC transistor of the other CML conducts for the other half. As shown in figure 3.9 a large capacitance isolates the DC level of the input clock from that of the MC gate. The DC level of MC gate is therefore determined by a biasing voltage, V_b. In order to improve the speed of the latch, this voltage can be set to a value slightly higher than Vdd. The biasing circuit which generates this voltage should have a large output resistance in order to minimize the clock signal power loss at this node.

The biasing circuit used in this block is a small inverter with shorted input/output as shown in figure 3.5. It contains a small inverter with its input and output shorted. Typical inverter output DC voltage is close to Vdd/2 in this configuration. In order to generate values higher than Vdd/2, the PMOS transistor can be made wider. Current consumption of such small inverter in this mode is relatively small. The output resistance of this inverter is the parallel connection of the PMOS and NMOS impedance which in this case is in the order of mega Ohms.

Cross-coupled ML transistors are used to store the outputs of the CML latch when the latch is in the hold mode. The most fundamental difference between dynamic and static dividers is the use of memory elements such as cross-coupled transistors or inverters in order to hold the output states. In dynamic dividers the output states only relies on the parasitics present at the output nodes. It will be shown later that cross-coupled inverters are used even in dynamic configuration but for different purposes.

In this design both cross-coupled NMOS transistors and inverters are used to maintain the output in the hold state. In conventional configurations, an MC transistor is also present at the source of the ML transistors whose gate is connected to the complementary clock signal that drives the main MC transistor [19] [25]. This configuration is used in CML latches which contain tail current sources. When the main MC transistor is turned off in the hold state, the current of the latch goes through the cross-coupled transistors. Since the tail current source is removed in this design, the second MC transistor can also be removed. This will also decrease the loading of the input clock signal.

MD transistors can be enlarged for noise considerations. But since each CML latch is also the load of the other one, large MD transistors increase the capacitive load at output nodes.

3.2.1 Self Oscillating Frequency vs. Maximum Operating Frequency

Self Oscillating frequency is defined to be the divider's oscillation frequency when the full-rate clock amplitude and the clock's DC differential voltage are both set to zero [18]. Like any other oscillator, a negative gm is required to compensate for the losses in the latch which can be modeled with a resistor [17]. The condition for oscillation is shown in equation 3.1.

$$gm.R_p \geq 1 \tag{3.1}$$

The negative gm is provided by the ML transistors and R_p is mostly the resistance of the MP transistors [2]. The self-oscillating frequency depends on the output time constant which can be formulated as shown in equation 3.2.

$$f_{os} = \frac{1}{C_{tot}.R_p} \tag{3.2}$$

where C_{tot} is the total parasitics at the output which contains parasitics from ML, MD and load. So according to equation 3.2, larger MP and smaller ML transistors are required in order to have a higher self-oscillating frequency. On the other hand, these two approaches go against the oscillating necessary condition which requires larger ML transistors for enough gm and smaller MP transistors for less loss. So there is a limit for how much the maximum self-oscillation frequency can be increased.

Low input amplitude can be handled more robustly if the divider's input clock frequency is close to two times the self-oscillating frequency of the divider [18]. The closer these two frequencies are, the lower the input amplitude can be. In the ideal case where input frequency is exactly two times the self-oscillating frequency, the input amplitude can be as low as zero. The more these two frequencies are from each other, the more input amplitude is needed in order to lock the divider.

A minimum value for the input voltage amplitude can be for all of the input frequency range. It is important to make sure that the input amplitude is larger than its corresponding minimum value in all frequencies of the input clock.

If the input clock frequency is lower than $2f_{os}$ and the input amplitude is low or has long rise and fall times, there will be enough time for the divider to self-oscillate briefly in between. The resulting waveforms exhibit the half-rate clock interspured with bursts of high frequency oscillations. The more the input is close to a square waveform (smaller rise and fall time), the more it can be prevented to enter this area [18].

If the input clock frequency is much higher than $2f_{os}$, at some point even a full-swing input cannot bring the divider into the locking region. At a certain higher frequency, there is not enough time for the internal nodes of the latches to be charged or discharged. The divider cannot follow the input and the dividing operation fails.

Simulation Results

The simulation setup for the divide-by-2 frequency divider is shown in figure 3.10. In order to drive the high-frequency and low-frequency bands, a chain of inverters are used as buffers

to drive the rest of of the dividing path. The first inverter is self-biased since the DC level of the CML-based frequency divider is not reliable to keep the inverters in their linear region. This inverter is chosen to be small enough in order to prevent overloading the divider and degrading divider's phase noise, and big enough to be able to drive the next inverters and have lower noise floor.

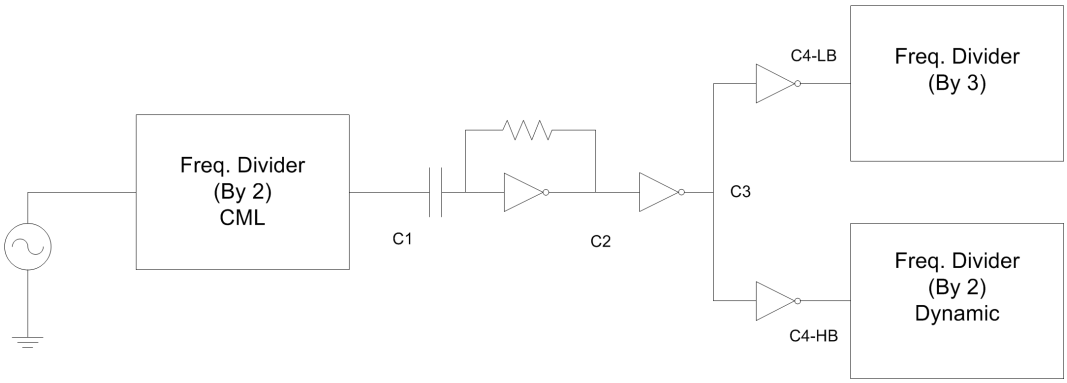

Figure 3.10: Simulation setup for the CML-based divide-by-2 frequency divider.

The Transient responses of the divider and the inverters are shown in figure 3.11.

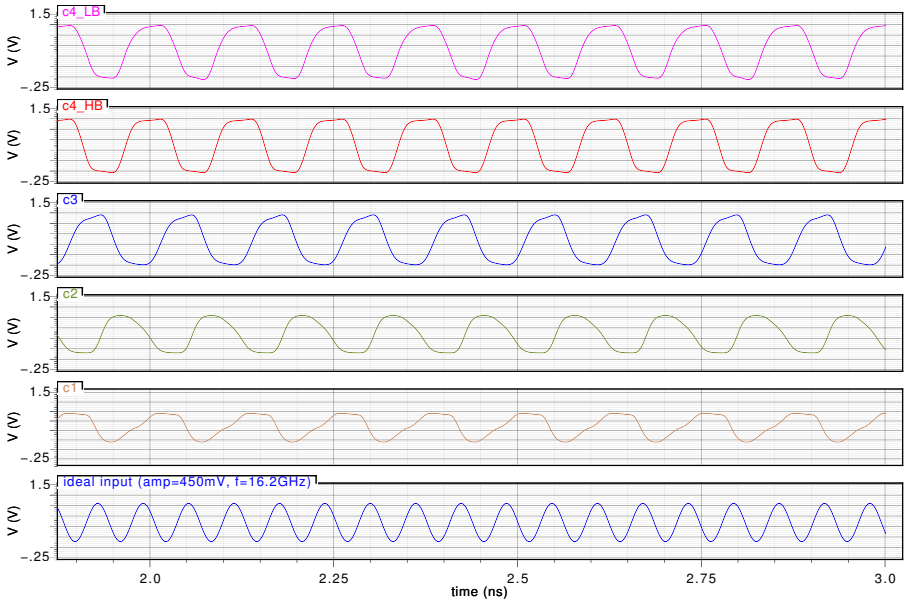

Figure 3.11: Transient response of the CML-based divider with an ideal source (DC=600 mV, amp=450 mV, freq=16.2 GHz).

The phase noise plots are shown in figure 3.12 and 3.13 for two different frequencies of interest. It can be seen how the inverter degrade the phase noise through the path. However, the use of these inverters is inevitable since the loading of the next dividers require a strong driving buffer.

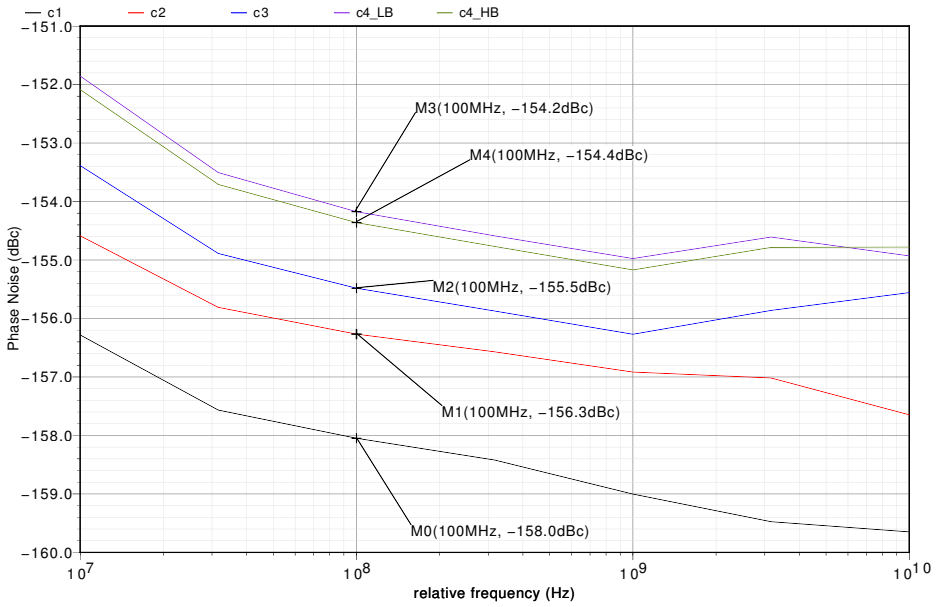

Figure 3.12: Phase noise plots for different nodes in figure 3.10 (DC=600 mV, amp=450 mV, input-freq=16.2 GHz).

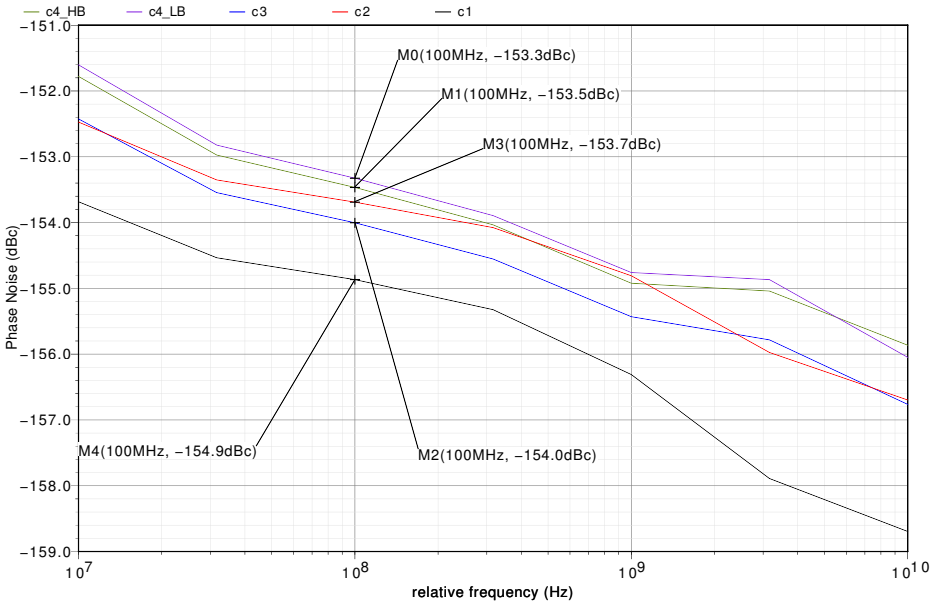

Figure 3.13: Phase noise plots for different nodes in figure 3.10 (DC=600 mV, amp=300 mV, input-freq=13.2 GHz).

3.3 Divide-by-3 Frequency Divider

As previously mentioned, the low-band path of the local oscillator consists of a divide-by-3 frequency divider and a frequency doubler. When cascaded, these two blocks form a divide-by-1.5 frequency divider. Local divide-by-2 frequency dividers will complete the act of dividing by 3 to generate the low-band frequencies.

As it will be discussed in section 3.4, the frequency doubler is a gate-based digital block which requires I/Q signals with %50 duty cycle as its inputs. This requirement originates from the basic functionality of the frequency doubler as illustrated in figure 3.26. The outputs of the divide-by-3 frequency divider contain four sets of falling and rising edges per one cycle with 90 degrees phase difference. The frequency doubler receives these four sets of edges at its input in order to produce a doubled-frequency differential signal with %50 duty cycle.

The main challenge in designing a divide-by-3 frequency divider is to meet the two important specifications: quadrature outputs with %50 duty cycle. Conventional flipflop-based frequency dividers are mainly designed to produce differential signals. In order generate quadrature outputs, two set of synchronized dividers are needed. Each dividing block uses eiher the I component or the Q component of the input clock signals. These two dividing

paths have to be synchronized in a way that their differential outputs have 90 degrees phase difference in order to have quadrature outputs.

3.3.1 Divide-by-3 Frequency Divider: First Design

A divide-by-3 frequency divider is shown in figure 3.14. Three D flip-flops are cascaded and are triggered with the input clock signals. The first two flip-flops are triggered with the rising edge of the differential clock signal so they use *clk*. The third flip-flop is triggered with the falling edge and uses $\overline{clk}$. A three-input NOR gate is used to produce the first flip-flop input, and a two-input NOR gate and a two-input NAND gate are used to generate the differential outputs.

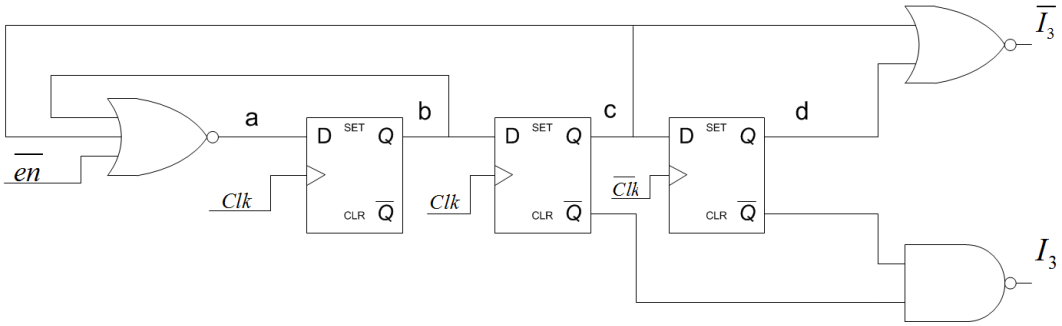

Figure 3.14: Schematic of the initial design of a divide-by-3 frequency divider.

In order to understand the performance of this divider, a timing diagram is shown in figure 3.15.

The enable signal, $\overline{en}$, is active low. When the enable signal is high, all the flip-flop outputs are low and the differential output is high. When the enable signal becomes low, *a* becomes high. As shown in figure 3.15, at the first rising edge of *clk* right after *a* becomes high, *b* becomes high and consequently *a* becomes low again. At the second rising edge, *c* becomes high and the outputs are changed for the first time. At the falling edge of the same clock cycle, the third flip-flop is clocked and *d* becomes high. It can be seen that either one of *c* or *d* signals are high for one and a half cycle of the input clock. The next rising edge of *c* also happens exactly one and a half cycle after the falling edge of *d*. Using NOR and NAND gates, the differential outputs can be produced with these two signals.

In order to generate quadrature outputs, another dividing block is needed to generate the second differential signal has 90 degree phase shift with the output of the first block. In order to synchronize these two dividing paths, the $\overline{en}$ of the second path is used to trigger the second block at the right clock edge. The complete divider is shown in figure 3.16

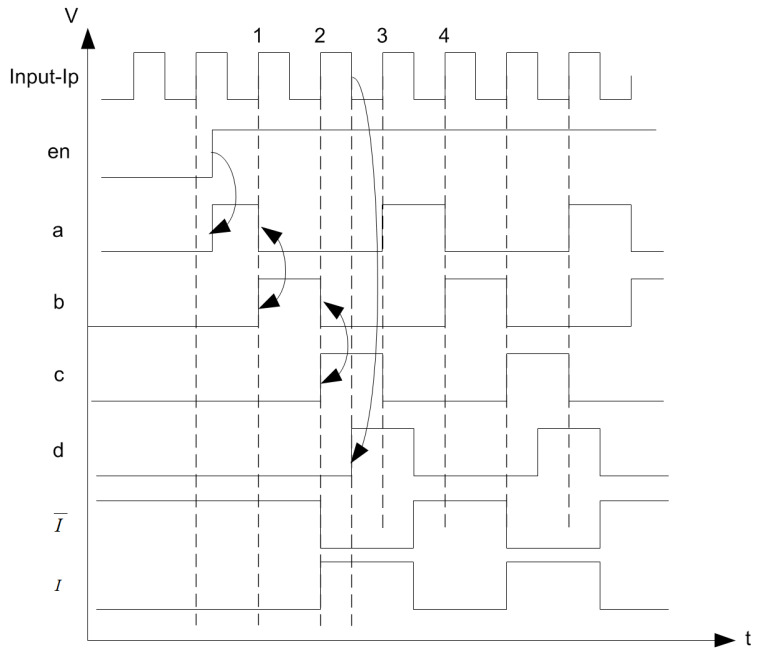

Figure 3.15: Timing diagram of the divide-by-3 frequency divider in figure 3.14.

The quadrature component of the input I/Q clock singals is used in the second dividing block. According to the timing diagram of figure 3.17, in order to have quadrature outputs, signal *b* of the second dividing path has to become high after 3/4 of the input cycle compared to the first block. This means that the first flip-flop of the second dividing block has to be triggered at the rising edge of $\overline{clk_Q}$ clock signal. The $\overline{en}$ input of the second block should also can also be the complementary value of the *b* signal of the first block which is the $\overline{clk_Q}$ output of the first flip-flop. In this way, the enable signal of the second path is not always low when active as the first block, but is only active when the *a* signal of the second path needs to be high before its corresponding $\overline{clk_Q}$ clock edge.

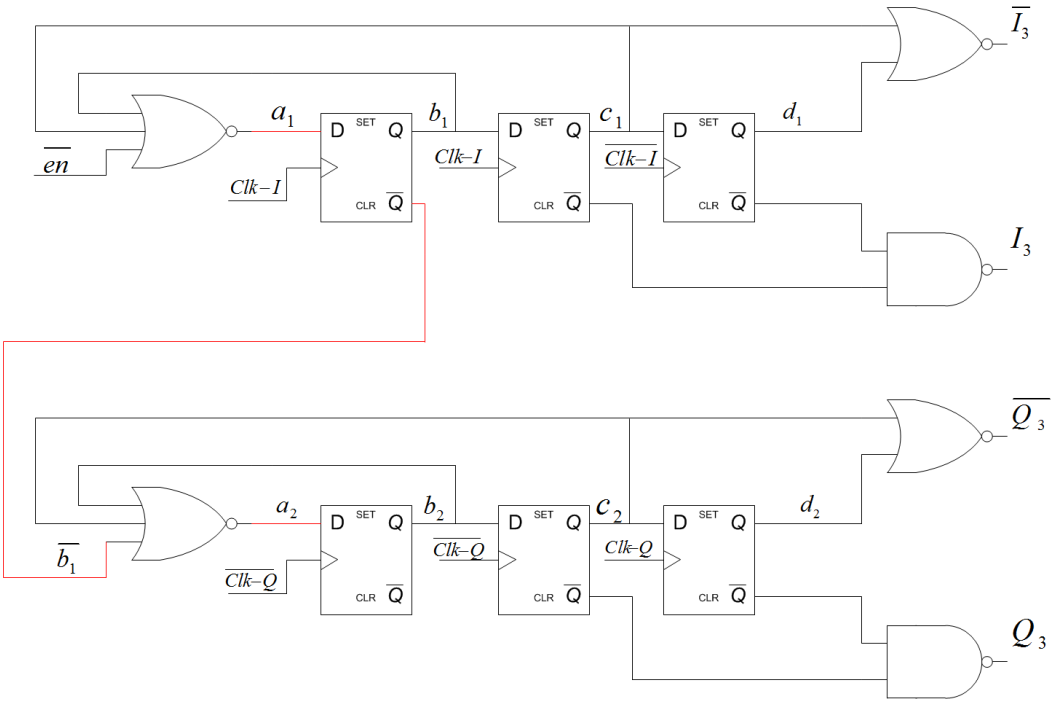

Figure 3.16: Complete divide-by-3 frequency divider to generate I/Q signals by using two dividing blocks of figure 3.14.

The most challenging part is the preparation of the second block $\overline{en}$ before its corresponding clock edge in each cycle. According to figure 3.17, b in the first block becomes high by the clk_I edge and a in the second block has to be low before the following rising edge of the $\overline{clk_Q}$ clock signal. The corresponding path between these two signals is highlighted in figure 3.16. This path contains the first flip-flop of the dividing path and the input NOR gate. Both of these blocks have delays which are comparable to the clock cycle. The sum of these two block delays need to be less than 3/4 of one input clock cycle.

The most important part of this design is the flip-flop. The input frequency of this divider is as high as 8.1 GHz according to frequency planning. This requires a fast flip-flop whose propagation delay is small compared to the input clock cycle. To reduce clock signal loading and handle the high frequency clock signals, edge-triggered dynamic flip-flops are a proper choice for this divider. A common form of dynamic flip-flops is the true single-phase clock (TSPC) flip-flops as shown in figure 3.18. This dynamic flip-flop performs with little power at high frequencies and only uses single phase clock signal. Having only 11 transistors makes it one of the fastest flip-flops which can be used in high frequency operations. Due to the dynamic nature of this flip-flop which means the outputs are stored in the parasitic capacitance rather than latches and other memory elements, this flip-flop may not work at certain low frequencies because leakage paths discharge the outputs in its long enough holding states.

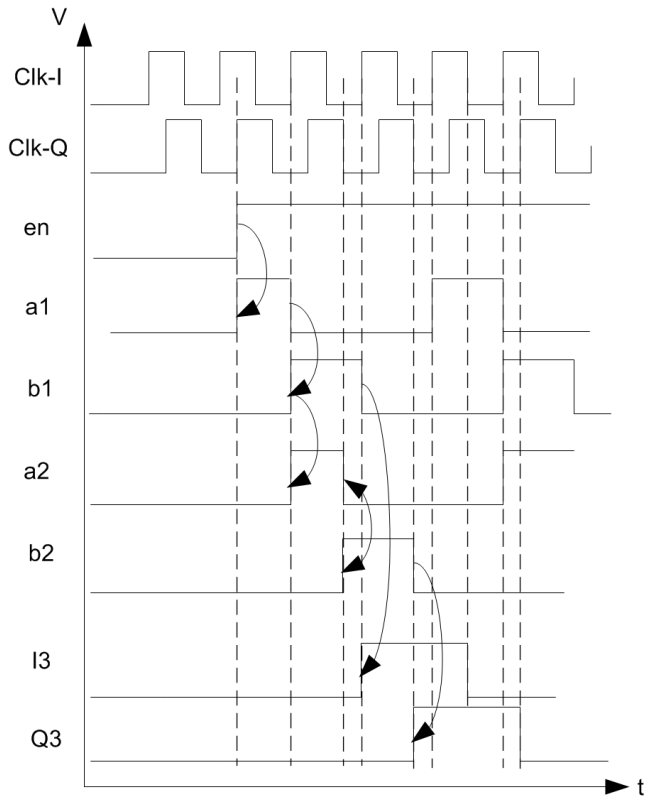

Figure 3.17: Timing diagram of the divide-by-3 frequency divider in figure 3.16.

When the clock signal is low, $MP3$ is switched on and y_2 is high. $\overline{Q}$ is connected to neither Vdd nor ground, which means that its value is determined by its previous charging state and this state is held by the parasitic present at node $\overline{Q}$. Node Q is determined consequently by the output inverter ($MP5$ and $MN6$). Assume the initial state of $\overline{Q}$ is high. At the next clock rising edge the value of the data signal will be copied to Q. Two different transitions are possible dependant of the data signal as follows:

1. $D = 1$: when data is high, $MN1$ is switched on and y_1 is connected to ground. When the clock signal becomes high, y_2 will not change because $MN2$ is still turned off. $MN4$ is switched on and $\overline{Q}$ is discharged to the ground via the path of $MN4$ and $MN5$ which was already turned on. Consequently, the output becomes high.

2. $D = 0$: when data is low, $MP1$ and $Mp2$ are both on in the holding state so that y_1 is pre-charged to Vdd. When the clock signal becomes high, y_2 is discharged to ground via the path of $MN2$ and $MN3$. $Mp4$ is switched on and $\overline{Q}$ is charged to Vdd. Consequently, the output becomes low.

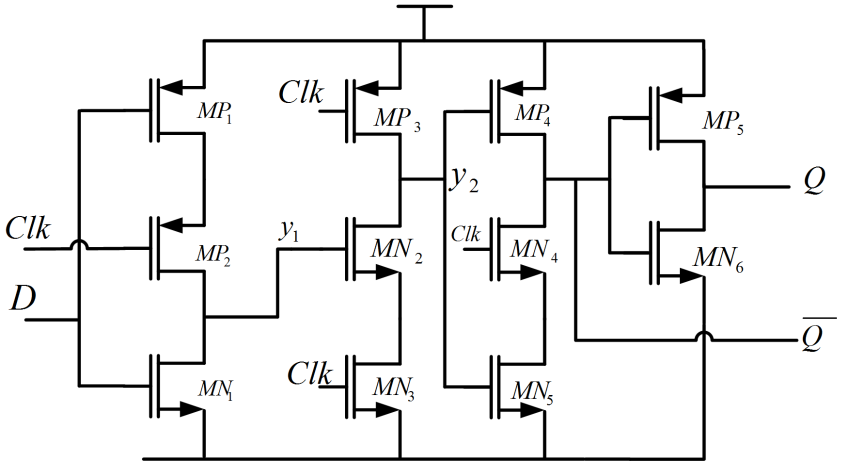

Figure 3.18: A true single-phase clock flip-flop

In the second transition, a small glitch can be visible at the output. This is due to the initial discharge of $\overline{Q}$ when the clock becomes high because y_2 is always pre-charged to Vdd before the clock rising edge. As soon as y_2 is discharged, $MP4$ will connect $\overline{Q}$ to Vdd.

The major drawback of the TSPC flip-flops is that due to its outputs asymmetry in relation to one another and also the high frequency of the signals, the error in output duty cycle will be a problem. In contrast with the differential and symmetrical topology of [14], for instance, the output complementary is generated via an inverter within the flip-flop. This will cause the differential outputs to have and error in their 180 degree phase shift. Due to high frequency of the outputs, this inverter delay generates a considerable error in output duty cycle.

There are other problematic parts in this divider which results duty cycle errors due to mismatch. The differential outputs are generated by two non identical gates. It is extremely difficult to make these two different gates have identical rising time, falling time and propagation delay under various mismatch conditions. Duty cycle correction circuits are also not an option in this design due to the complexity of the system and tight phase noise requirements.

3.3.2 Asynchronous Divide-by-3 Frequency Divider

After investigating several divide-by-3 frequecy dividers, an asynchronous divide-by-3 frequency divider is used in the final design as shown in figure 3.19 [4]. Asynchronous dividers are used to realize odd integer dividers such as divide-by-3 and divide-by-5 stages. Outputs of this divider stage are derived as a combinational logic function of the quadrature input and the quadrature output variables. Quadrature inputs with %50 duty cycle generate quadrature outputs with %50 duty cycle. This divider operates in CML mode and is area consuming due the load resistors and tail current mirrors. However, due to the low supply

voltage, the tail current mirrors are removed.

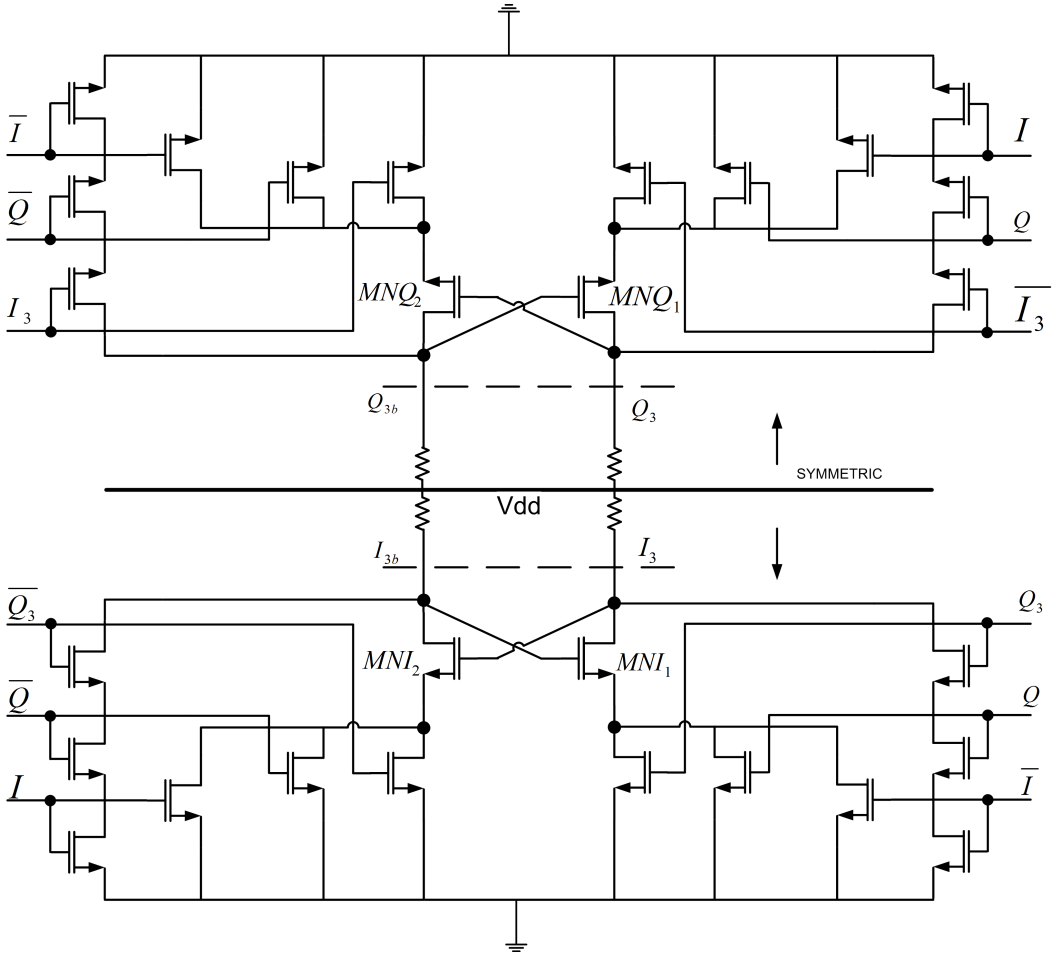

Figure 3.19: Schematic of a asynchronous divide-by-3 frequency divider [4].

The advantages of this divider are:

1. Capability to operate at high frequencies due to its CML nature.
2. Low power consumption compared to its synchronous counterparts by reducing activities at the high speed clock.
3. Reducing the loading of the clock signal compared to flip-flop-based dividers

The divider input-output timing diagram is shown in figure 3.20. The combinational logic formalism needed to set or reset the output signal in order to have divided-by-3 outputs with %50 duty cycle is shown below:

- I_3: $S = I.\overline{Q}.\overline{Q_3}$ $R = \overline{I}.Q.Q_3$
- Q_3: $S = \overline{Q}.\overline{I}.I_3$ $R = Q.I.\overline{I_3}$

Where I and Q are the I/Q input signals. Once the logic high and logic low of the outputs are determined, they are the input to an SR latch respectively to obtain the outputs. Finally the low-swing outputs are fed to self-biased buffers in order to be able to drive the next stage which is the frequency doubler.

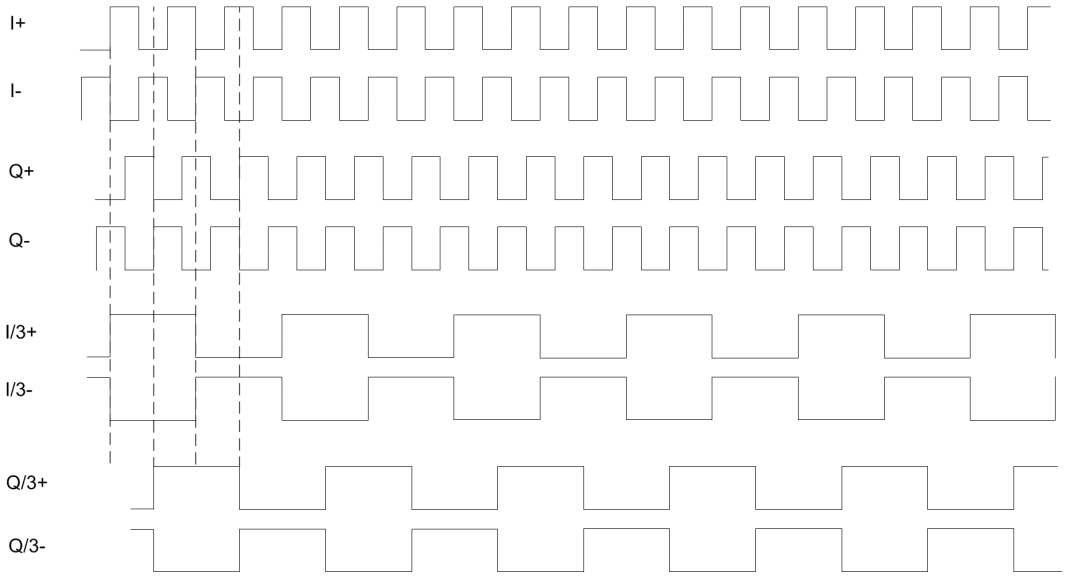

Figure 3.20: Timing diagram of the asynchronous divider in figure 3.19 [4].

As shown in figure 3.19, Cross-coupled pair of MNI_1/MNI_2 and MNQ_1/MNQ_2 are the SR latches which maintain the in-phase and quadrature-phase outputs of the divider respectively. The three cascoded transistors form the reset logic and pull down the output voltage. The combination of three parallel transistors and the pull-up resistor form the complementary set logic i.e. $S = I.\overline{Q}.\overline{Q_3} = \overline{\overline{I} + Q + Q_3}$.

At resetting time for I_3, the output is pulled down to ground via the three cascoded transistors of M_1, M_2 and M_3. This will turn off MNI_2, $\overline{I_3}$ will be pulled up to Vdd via the load resistor and MNI_1 starts to turn on. I_3 will be kept low via MNI_1 and three parallel transistors at MNI_1 source. The parallel transistors will always provide a path to ground except for the setting time of their corresponding output i.e. when $\overline{I_3}$ is resetting.

During setting time, the pull-up resistor provides the path to Vdd. Output rising slope is then dependent on this resistor, the parasitic capacitances of the output node and the divider capacitive output load.

Simulation Results

The simulation setup for the divide-by-3 frequency divider is shown in figure 3.21.

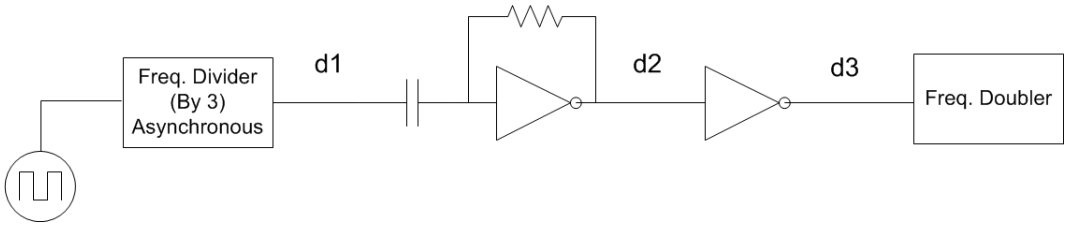

Figure 3.21: Simulation setup for the asynchronous divide-by-3 frequency divider.

Due to the insufficient output swing to drive the next stage, a buffer is used to generate full swing signals. The same buffer as used for the static divide-by-2 frequency divider in section 3.2 is used for this stage as well. As it is shown in figure 3.21 the first inverter is AC-coupled to the outputs of the divider. Inverters contribution to the noise floor is negligible and full-swing I/Q signals will assure the high-frequency performance of the frequency doubler with low noise floor.

The transient response of the output signal of the divider is shown in figure 3.22.

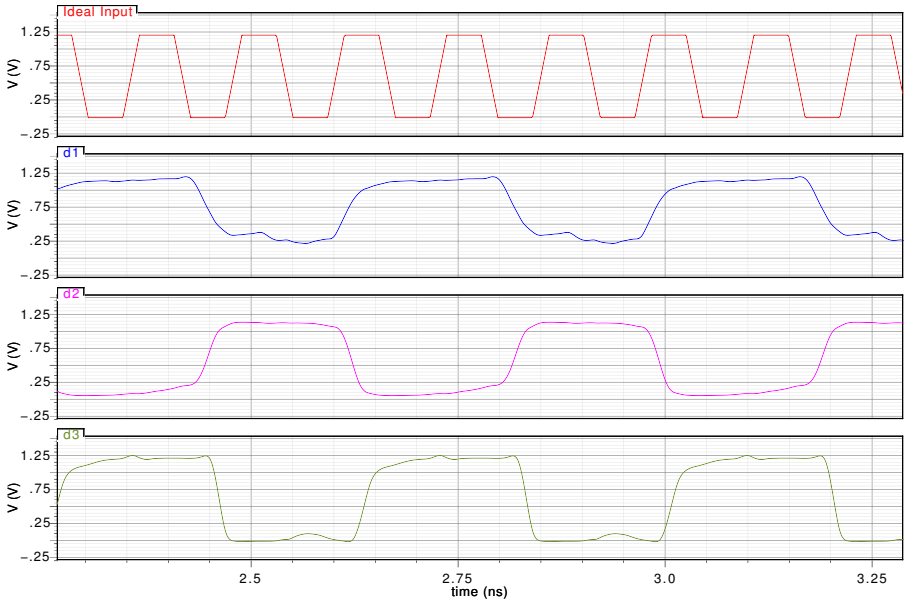

Figure 3.22: Transient response for the schematic of figure 3.21 at f=16.2 GHz.

Phase noise simulation results for different nodes in 3.21 is shown in figures 3.23 and 3.24.

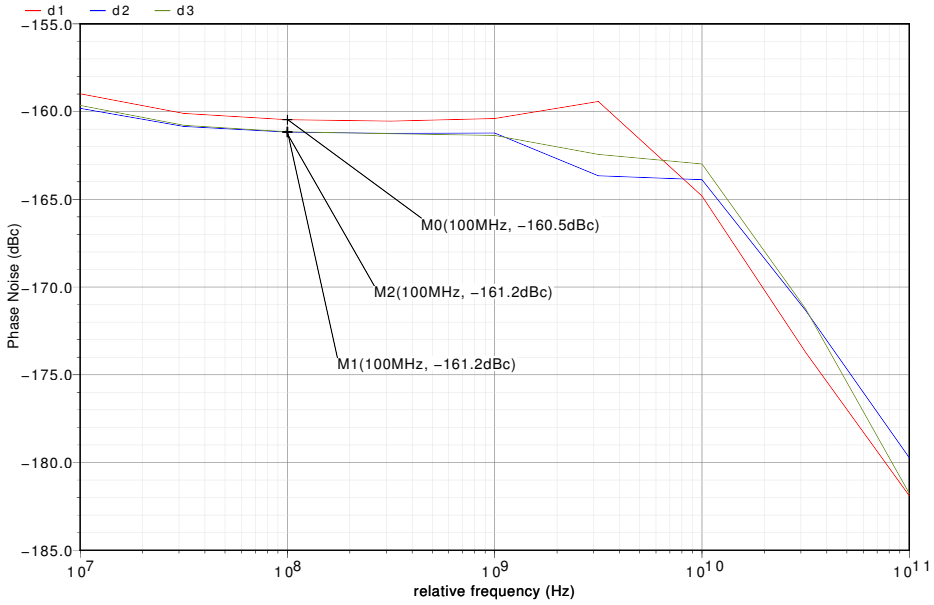

Figure 3.23: Phase noise plot for the schematic of figure 3.21 at f=16.2 GHz.

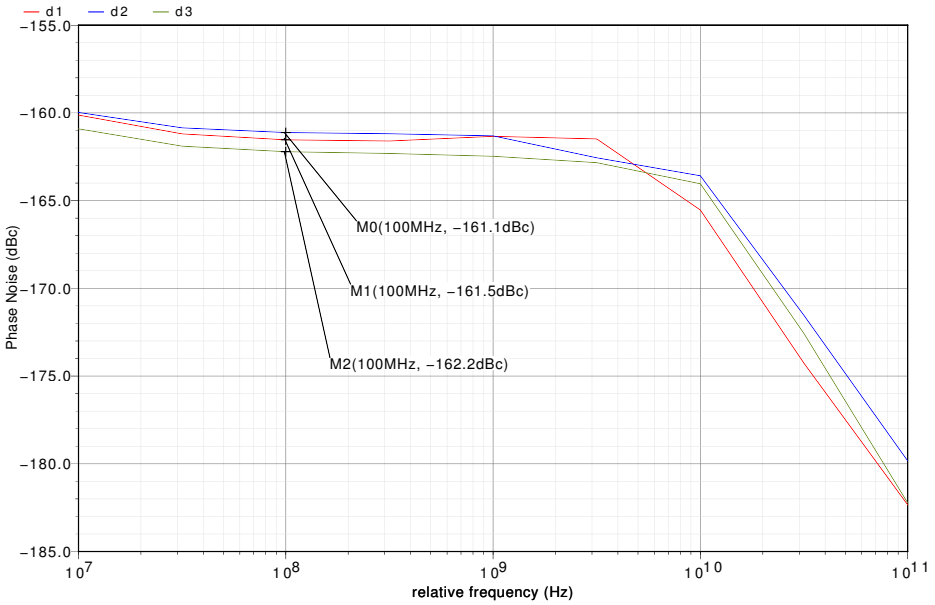

Figure 3.24: Phase noise plot for the schematic of figure 3.21 at f=13.2 GHz.

3.4 Frequency Doubler

Placing the final divide-by-2 frequency dividers at the end of the routing close to the transceiver provides excellent I/Q balance for all division ratios. It also allows the routing of the signal in differential phases instead of quadrature which is more area-efficient. Since two dividing block with division ratios of 2 and 3 have already completed the divide-by-6 frequency division in the low band, the extra division by two must be compensated by a frequency doubler in this path.

Implementing a divide-by-3 frequency divider which generates quadrature outputs, allows the following frequency doubler to be easily implemented using the XOR function as shown in equation 3.3. As shown in figure 3.25, when two clock signals with %50 duty cycle and 90 degree phase shift are the inputs of an XOR gate, the output has double the frequency of the inputs with %50 duty cycle.

$$Out = A \bigoplus B = A.\overline{B} + \overline{A}.B \tag{3.3}$$

According to equation 3.3, an XOR gate can be implemented using a 2-to-1 multiplexer. The data inputs and the selecting signals are both differential and have 90 degrees phase shift.

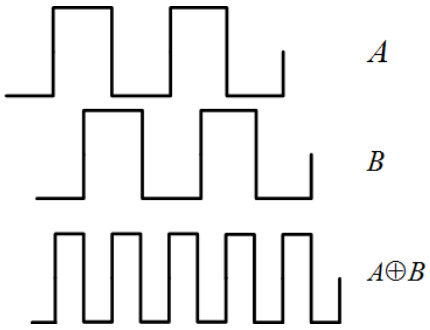

Figure 3.25: XOR function and frequency doubling.

In order to generate differential outputs with double the frequency, two multiplexers are used as depicted in figure 3.26. Data signals have 90 degree phase shift with the selecting signals in both multiplexers. According to equations 3.4 and 3.5, the input clock signals and their corresponding selective values are determined. Based on these equations, the frequency doubler can be implemented as shown in figure 3.26.

$$Out = I \bigoplus Q = I.\overline{Q} + \overline{I}.Q \tag{3.4}$$

$$\overline{Out} = \overline{I} \bigoplus Q = \overline{I}.\overline{Q} + I.Q \tag{3.5}$$

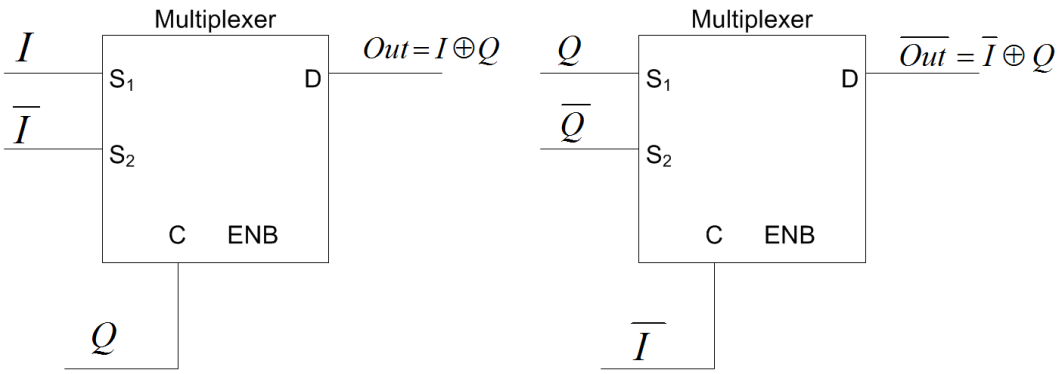

Figure 3.26: Frequency doubler consisting of two multiplexers.

Each multiplexer input is differential and the selecting signal is a single-phase clock signal with 90 degrees phase shift in relation to the input data.

Each Multiplexer is implemented using two transmission gate as depicted in figure 3.27.

Each Transmission gate consists of an NMOS and an PMOS connected in parallel and their gates connected to the selecting signals. The output of the multiplexer can be modeled

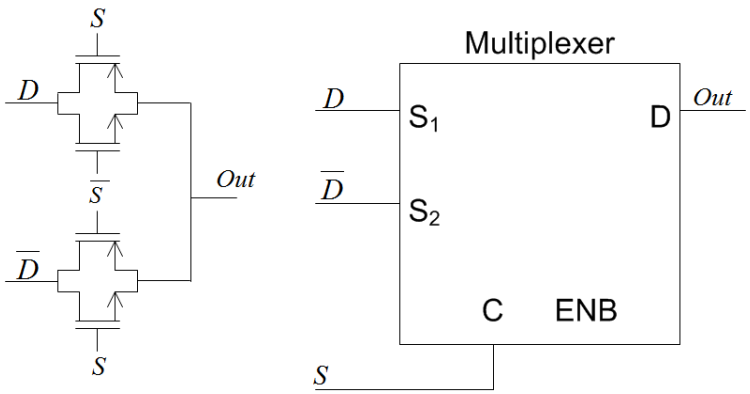

Figure 3.27: Schematic of a 2-to-1 multiplexer.

with a capacitor. This capacitor contains the parasitics of the transmission gate output terminal and the load capacitor. In order to drive the next stage, the output of the multiplexer is fed to an inverter which provides a clean amplified signal. The final schematic of the frequency doubler is shown in figure 3.28.

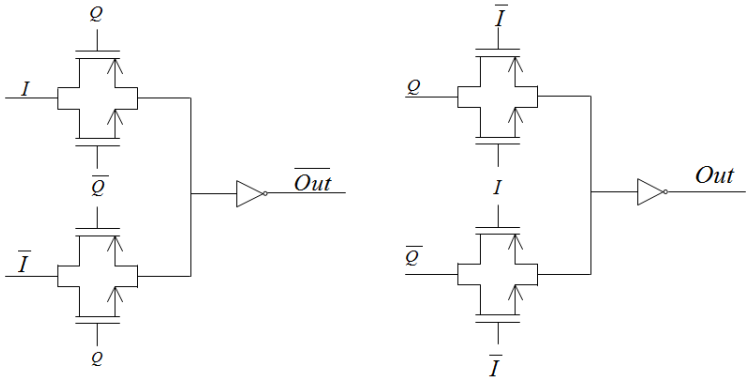

Figure 3.28: Complete schematic of the frequency doubler.

Due to the high frequency operation of the frequency doubler, symmetry of the two blocks are necessary in order to generate differential outputs with %50 duty cycle. Any mismatch between the two multiplexing paths or any layout asymmetry results in phase mismatch and duty cycle error respectively.

Simulation Results

The simulation setup for the frequency doubler is shown in figure 3.29 with the final divide-by-2 frequency divider as its load.

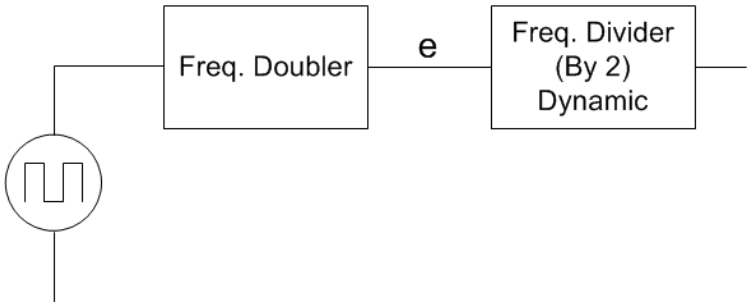

Figure 3.29: Simulation setup for the frequency doubler.

The transient response of the frequency doubler is shown in figure 3.30.

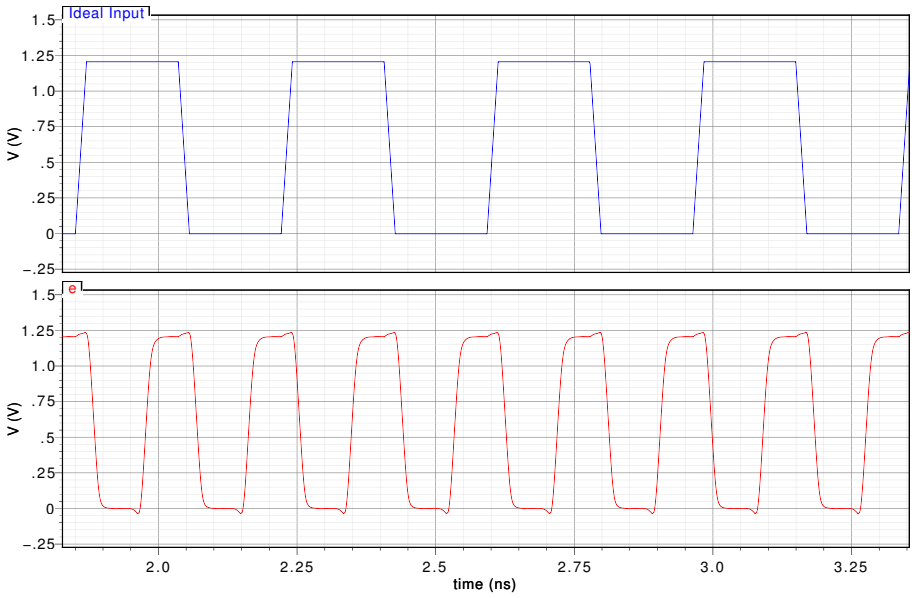

Figure 3.30: Frequency doubler transient response.

Due to the simple schematic of the frequency divider and low resistive path for the clock signals which is mostly due to the transmission gate ON resistance, low noise floor can be achieved at the outputs. The Phase noise plot of the frequency divider driven by ideal sources is depicted in figure 3.31.

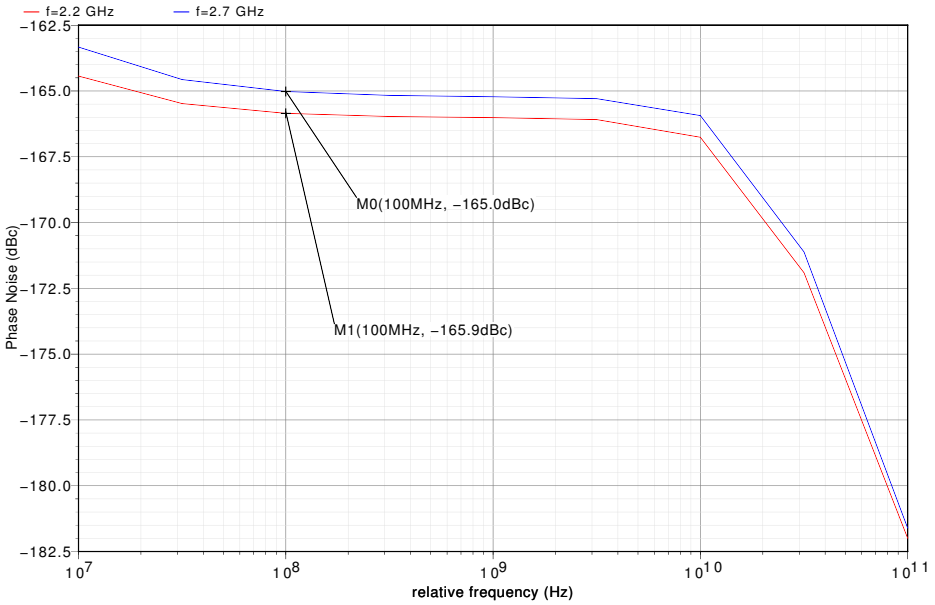

Figure 3.31: Frequency doubler phase noise plots

3.5 Dynamic Divide-by-2 Frequency Divider

The final dividing block in both dividing paths is a dynamic divide-by-two frequency divider. As mentioned before, the only reason that this divider is not used in the first divide-by-two dividing block is its lower maximum operating frequency compared to CML-based dividers with low-swing clock inputs. At the end of the dividing chain, however, the operating frequency is lower and this low-power low-noise dynamic divider is much more suitable.

The schematic of the dynamic divider used in this design is shown in figure 3.32. The divider contains four transmission gates and four inverters connected in a loop. Each transmission gate is controlled by the differential input clock signals. Only two transmission gates are conducting in each half of the clock period. Disregarding the cross-coupled inverters at the outputs, the output state is stored in the parasitics in the output which mostly consists of drain/source parasitics of the next transmission gate. It can be realized that any output leakage can change the output state after a certain time depending on leakage paths. So at some certain low frequency, the parasitics are not sufficient to store the output data and the divider performance is disturbed. This means that aside from a maximum operating frequency, a minimum operating frequency is also defined for dynamic dividers or any divider which possesses a dynamic nature.

The small cross-coupled inverters between differential outputs can be realized as a mem-

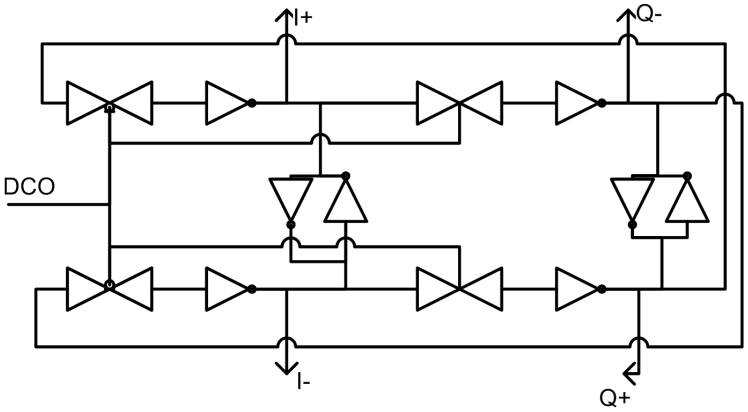

Figure 3.32: Schematic of the dynamic divide-by-two frequency divider.

ory element which exists at the outputs. But the main purpose of these inverters is not their latching functionality but the divider start-up. Bigger inverters can start up the divider faster. There is a limit for how small these inverters can be and at some point the divider stops functioning for smaller inverters. Although sizing up the inverters shortens the start-up time of the divider, their capacitive load is directly added to the outputs total load and degrades the output noise floor. So moderate-sized inverters which guaranty divider's start-up are sufficient.

The most important design parameters which determine the noise performance and the maximum operating frequency of the divider are transmission gates and inverters sizes. Large transmission gates provide low resistance in the path of the signal when the transmission gate is conducting. On the other hand, larger transmission gates introduces larger capacitive load to the input clock signals.

The inverters input capacitances contribute to the total time constant of signal propagation delay through the transmission gates. On the other hand, in order to improve the output noise floor, these inverters need be sized up.

The most important characteristic of this dynamic divider is the full-swing output signals results in very low noise floor. At this point of the divider chain, enough clock amplitude is provided which guarantees the performance of the divider.

Simulation Results

The simulation setup is shown in figure 3.33. The load is estimated as 20fF.

The transient response and the phase noise plot for the output of the divider is shown in figures 3.34 and 3.35 respectively.

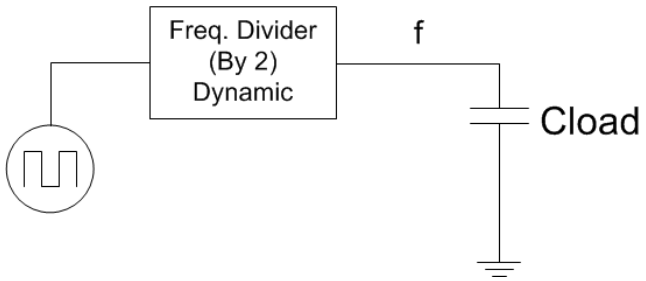

Figure 3.33: Simulation setup for the dynamic divide-by-2 frequency divider.

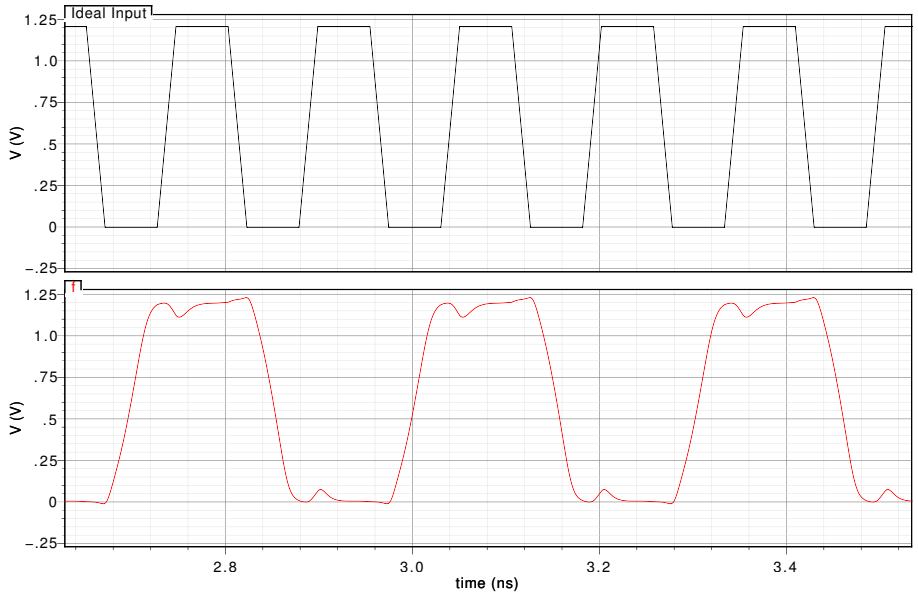

Figure 3.34: Transient response of the dynamic divider.

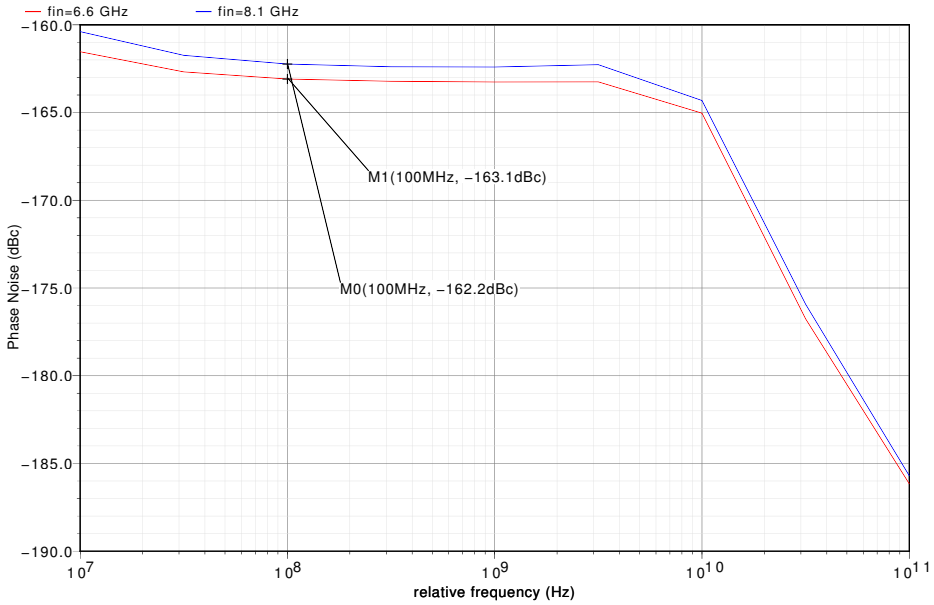

Figure 3.35: Phase noise of the dynamic divider.

Chapter 4

Post-Layout Simulation Results: Discussion and Conclusion

This chapter is mainly dedicated to the final simulation results. In RF circuit design, the traditional trend of schematic simulation, layout implementation, parasitic extraction and post-layout simulation is not a unilateral trend. Post-layout simulation results often make the designer modify the original schematic design in different iterations in order to find the optimal spot. Phase noise results often change dramatically in post-layout simulations, as well as capacitor banks with linear transfer functions which require numerous iterations in order to have minimized linearity deviation. Therefore, it is important to look at RF schematics and layouts as two inseparable design processes.

The final extracted results are listed in this chapter. Capacitor bank, DCO core and frequency dividers are the main designed blocks. The results are analyzed and discussed and finally a conclusion is made regarding the total approach and implementation.

4.1 PVT Bank

Table 4.1 shows the final specifications of the PVT varactors. Seven binary-weighted varactors are implemented to cover the tuning range of the DCO core. Table 4.1 shows each varactor's capacitance in ON and OFF state and the ΔC of each varactor.

The quality factor of the PVT bank after parasitic extraction is shown in figure 4.1. It can be seen that the quality factor degrades when shifting to lower frequencies.

The transfer function of the PVT bank is shown is figure 4.2 in different process corners. The transfer function is the capacitance of the PVT bank versus the control word. It can be seen that in different process corners, the slope of the transfer function plot is changed but the linearity of the plot is not disturbed.

Table 4.1: Final output parameters of the PVT Bank varactors.

Number	$C_{min}(fF)$	$\Delta C(fF)$
1	1.9	2.4
2	2.4	4.8
3	4.0	9.6
4	8.0	19.2
5	13.1	38.4
6	27.5	76.8
7	53.0	153.6

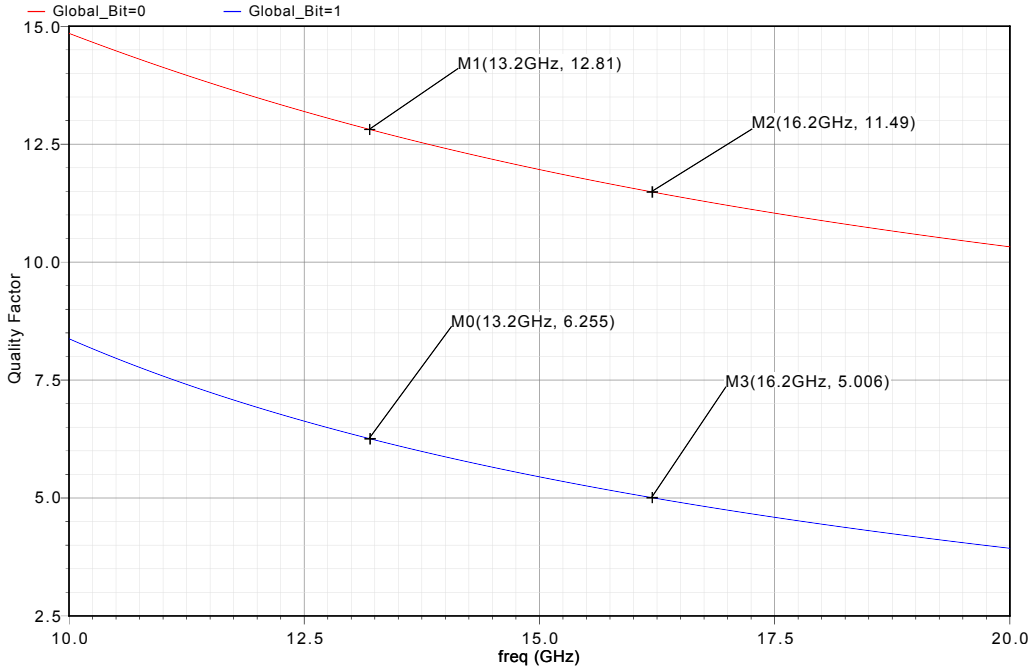

Figure 4.1: Quality factor of the PVT bank for the ON and OFF states after parasitic extraction.

The fixed error of the PVT bank capacitance steps is less 0.45 fF in typical process corner which is less than 0.2 times the least significant capacitance step. For the most critical step of the PVT bank where the control word changes from 63 to 64, Monte Carlo simulations for mismatch variations show that the variation (σ) of this particular ΔC is less than 120 aF.

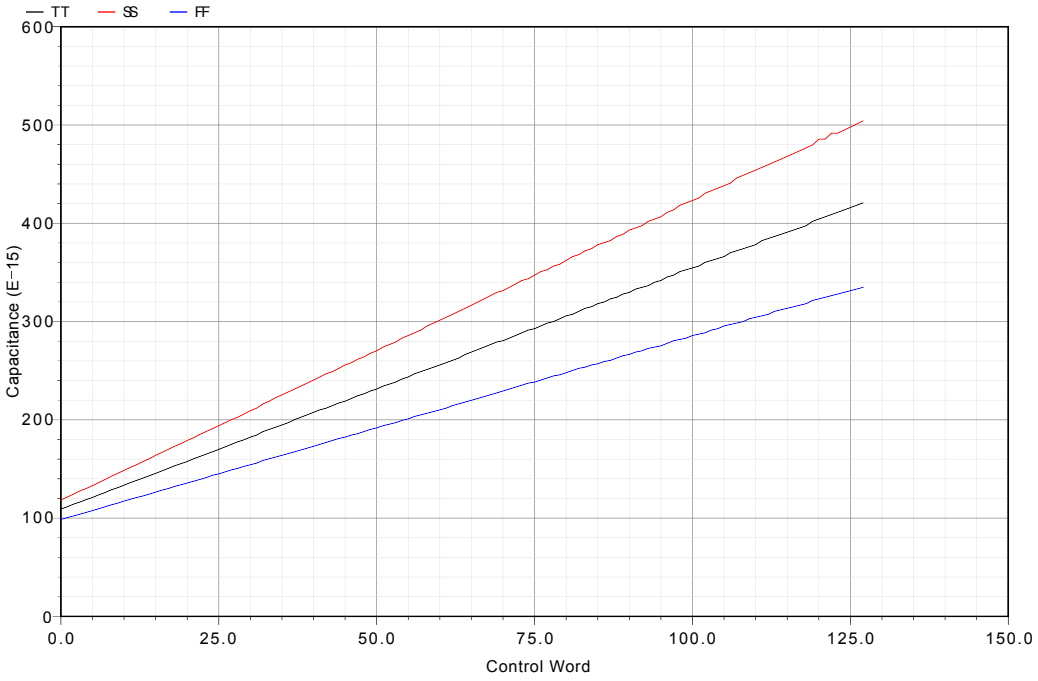

Figure 4.2: Transfer function of the PVT bank in different process corners.

4.2 Acquisition Bank

Table 4.2 shows the final specifications of the AB varactors. Six binary-weighted varactors are implemented in acquisition bank. Table 4.1 shows each varactor's capacitance in ON and OFF state and the ΔC of each varactor. The quality factor of the acquisition bank after parasitic extraction is shown in figure 4.1

Table 4.2: Final output parameters of the acquisition bank varactors.

Number	$C_{min}(fF)$	$\Delta C(aF)$
1	1.43	160
2	1.87	320
3	2.42	640
4	3.15	1280
5	4.23	2560
6	5.67	5120

The Transfer function of the acquisition bank is shown is figure 4.4 in different process

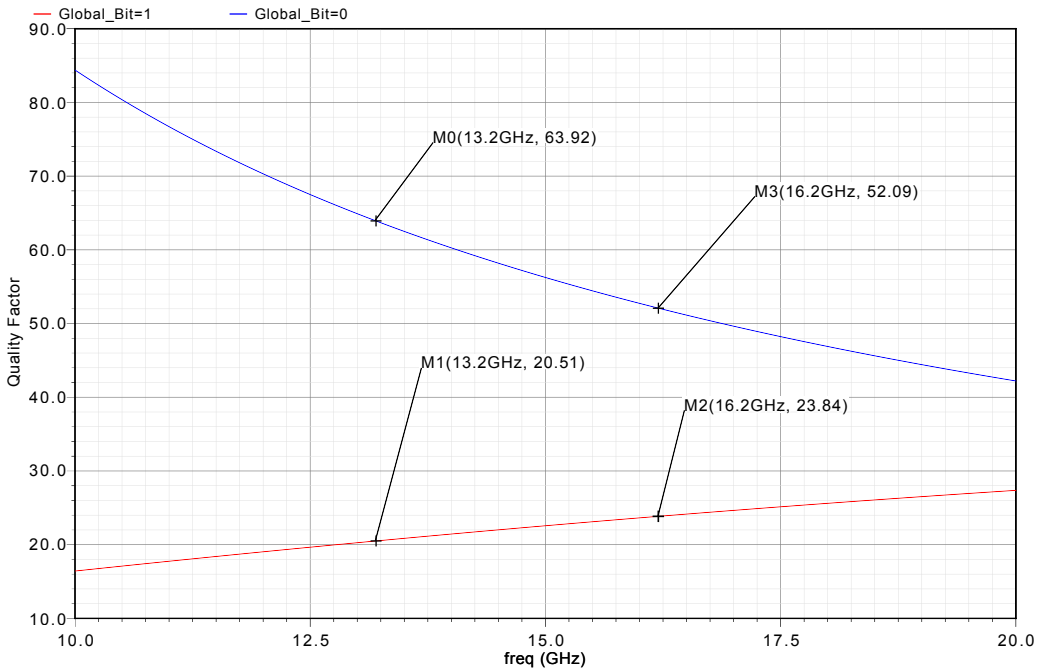

Figure 4.3: Quality factor of the acquisition bank for the ON and OFF states after parasitic extraction.

corners. As shown for PVT bank, it can be seen that in different process corners, the slope of the transfer function plot is changed but the linearity of the plot is not disturbed.

The fixed error of the acquisition bank capacitance steps is less 40 aF in typical process corner which is less than 0.3 times the least significant capacitance step. For the most critical step of the acquisition bank where the control word changes from 31 to 32 , Monte Carlo simulations for mismatch variations show that the variation (σ) of this particular ΔC is less than 15 aF.

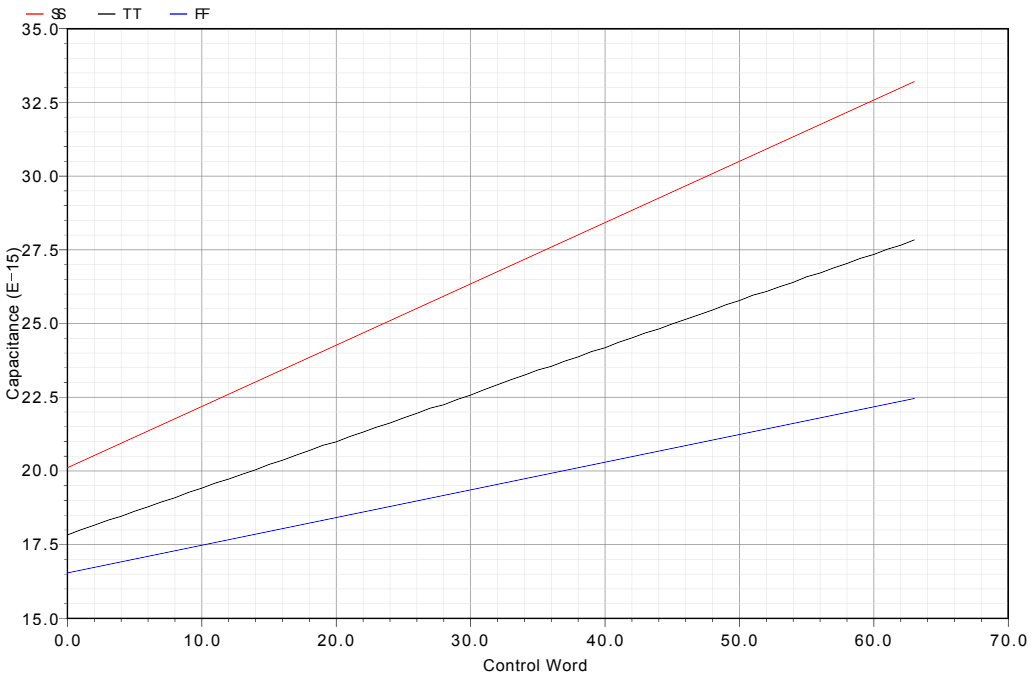

Figure 4.4: Transfer function of the acquisition bank in different process corners.

4.3 Tracking Bank

The transfer function of the tracking bank varactor is shown in figure 4.5. The fixed post-layout error is less than %5. The capacitance step of the tracking bank is shown in table 4.3.

The quality factor of the tracking bank is shown in figure 4.6. This figure can be compared to figure 2.36 and see how the quality factor is degraded due to the long interconnections in the layout.

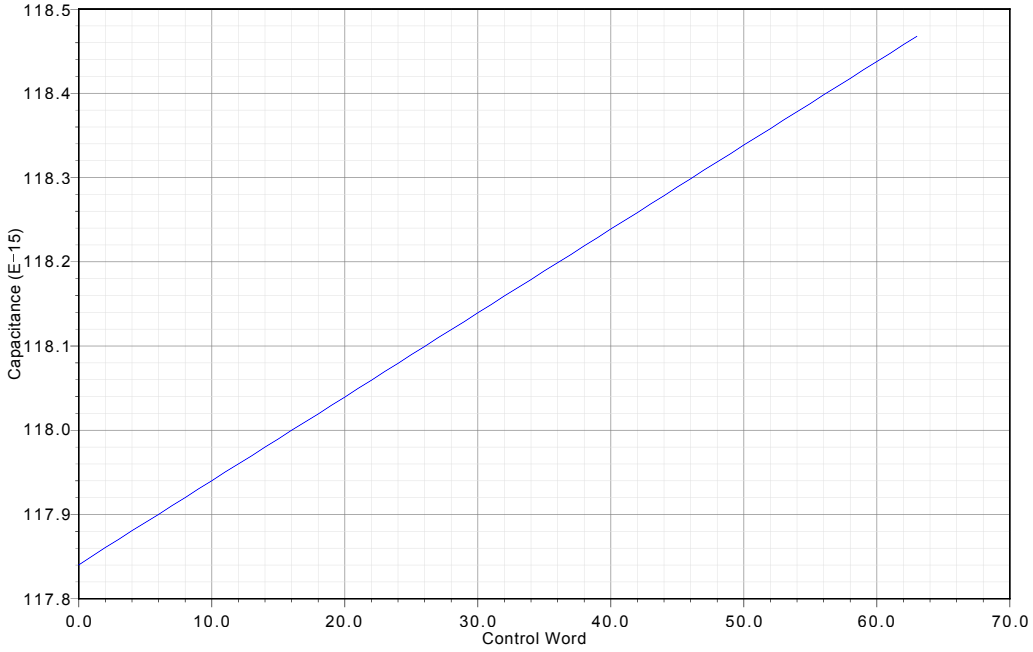

Figure 4.5: Transfer function of the tracking bank in the typical corner.

Table 4.3: Capacitance steps of the tracking bank varactors in different process corners.

Process Corner	$C_{min}(fF)$	$\Delta C(aF)$
tt	0.89	9.5
ss	1.06	11.6
ff	0.72	7.4

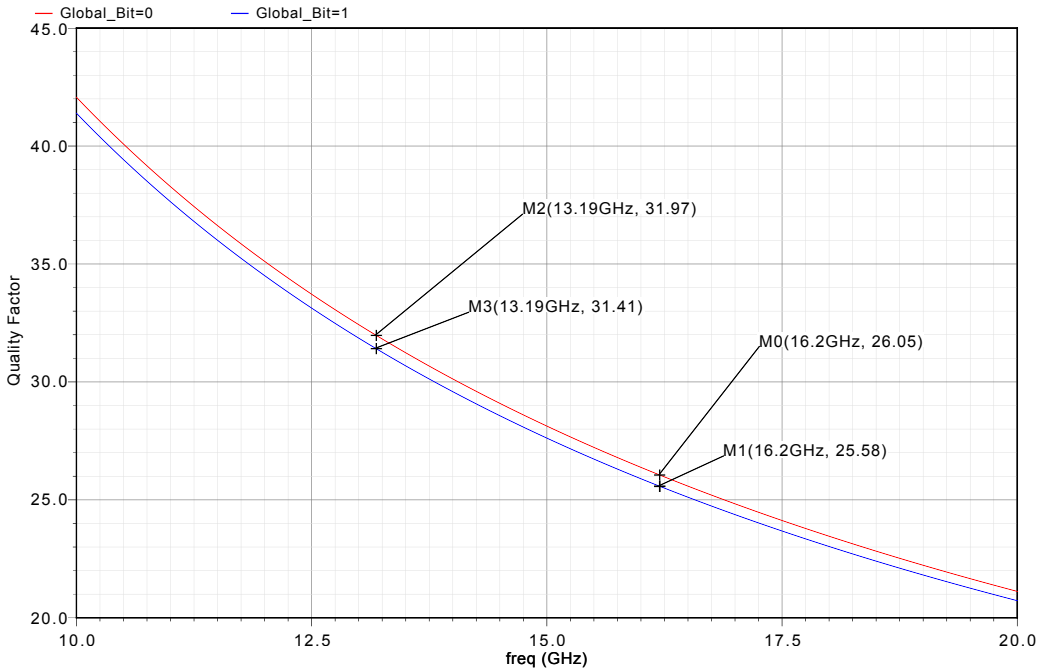

Figure 4.6: Quality factor of the tracking bank after parasitic extraction.

4.4 Post-Layout Phase Noise Simulations: Frequency Dividers

Figure 4.7 shows the final DCO system architecture used in phase noise simulations. Frequency division improves the phase noise 3 dB per each divide-by-2 frequency division. On the other hand, cascaded buffering inverters also contribute to the long dividing paths and makes it quite challenging to meet the required specification of less than -150 dBc/Hz at far-out phase noise.

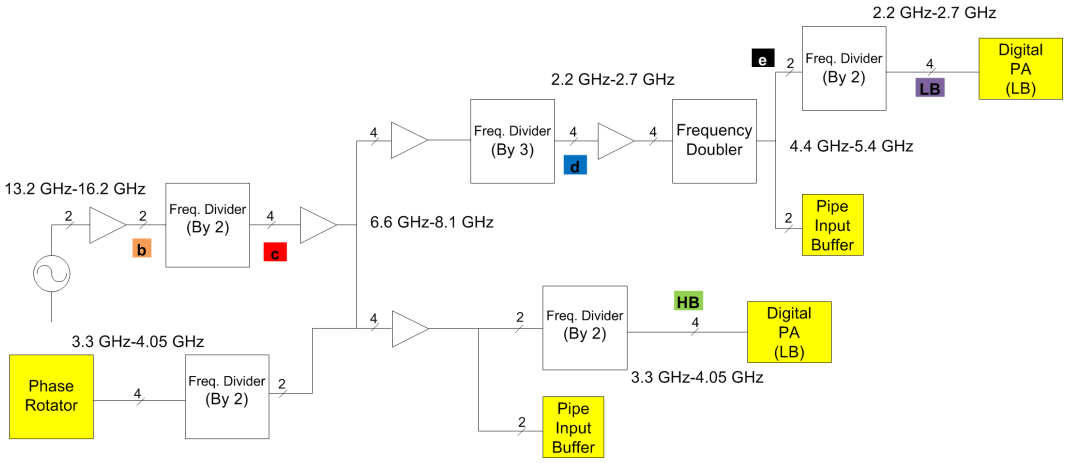

Figure 4.7: Final DCO system architecture and the simulation setup.

Figures 4.8 and 4.9 show the post-layout phase noise simulation results for $f_{max} = 16.2\ GHz$ and $f_{min} = 13,2\ GHz$. The power consumption of different blocks is shown in table 4.4.

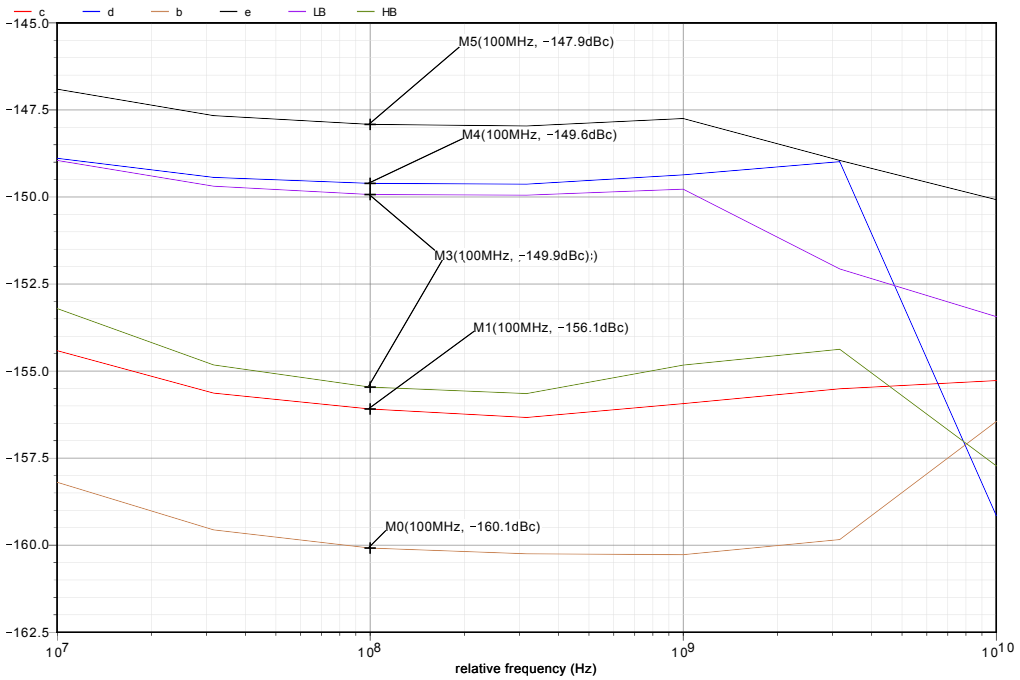

Figure 4.8: Post-layout phase noise simulation results for different nodes in figure 4.7 at f=16.2 GHz.

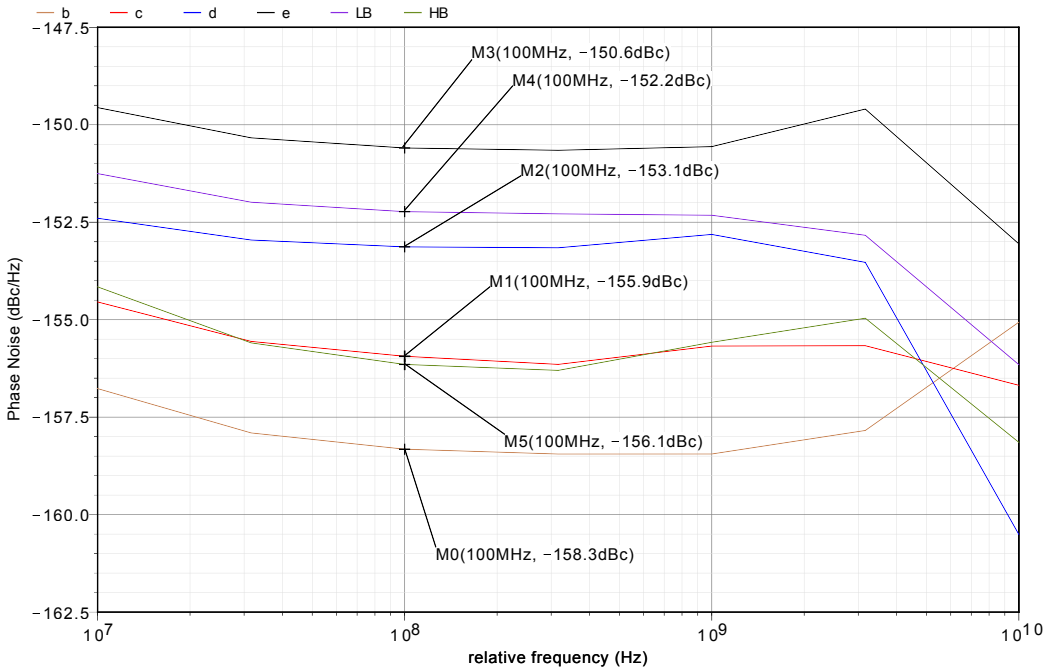

Figure 4.9: Post-layout phase noise simulation results for different nodes in figure 4.7 at f=13.2 GHz.

Table 4.4: Power consumption of all the dividing blocks

Block	I_{avg}(mA) at f= 16.2GHz	I_{avg} (mA) at f=13.2 GHz
DCO Buffers	1.3	1.1
CML Divider	2.8	2.7
CML Divider Buffers	4.1	3.7
Divider by 3	3.9	3.7
Divider by 3 Buffers	1.5	1.3
Frequency Doubler	0.4	0.3
Dynamic Divider LB	0.9	0.8
Dynamic Divider HB	1.4	1.3
Total	16.3	14.6

4.5 Post-Layout Phase Noise Simulations: DCO system

The phase noise requirements defined by the ADPLL design is shown in table 4.5 [16], [12], [6].

Table 4.5: Phase Noise requirements of the DCO system.

frequency offset	at 3.8 GHz (dBc/Hz)	at 3.3 GHz (dBc/Hz)
10 KHz	-72.3	-71.7
100 KHz	-98.9	-98.0
10 MHz	-140.9	-140.2
500 MHz	-150	-150

The period steady-state simulation shows the final frequency range of the DCO core and the low and high frequency bands as shown in figure 4.10.

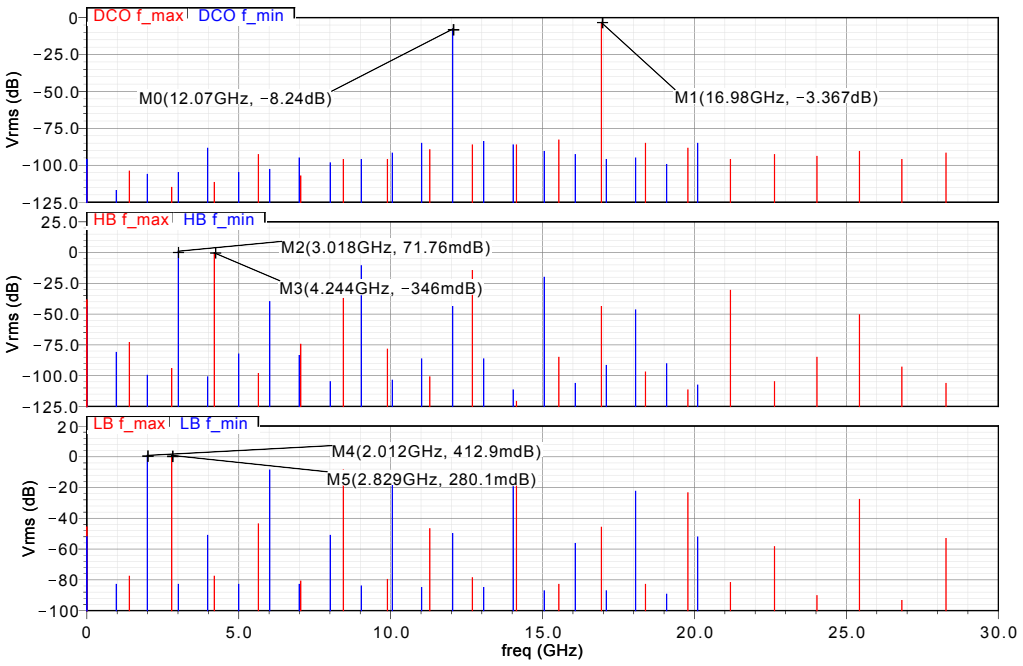

Figure 4.10: Periodic steady-state of the DCO core: the high frequency band (HB) and the low frequency band (LB). For this simulation, LB path is without any load.

The phase noise simulation results of the DCO system at the high-frequency band is

shown in figure 4.11. For the low-frequency band, the phase noise plots are shown in figure 4.12 and 4.13 for f_{max} and f_{min} of the low band respectively. It can be seen that noise floor is larger than -150 dBc/Hz in the maximum frequency of the low band.

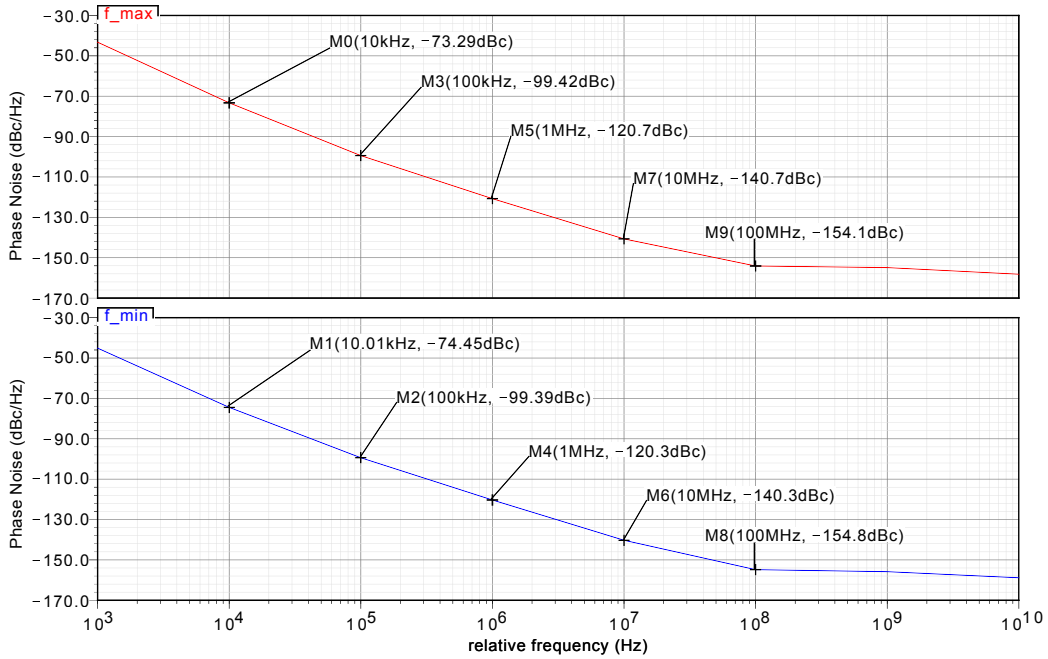

Figure 4.11: Post-layout phase noise simulation result of the DCO system in low-band frequencies.

Transient response of the DCO system is shown in figure 4.14. The current consumption of the DCO core is 3.54 mA and 3.40 mA for f_{max} and f_{min} of the DCO core respectively. DCO core DC current is 2.45 mA.

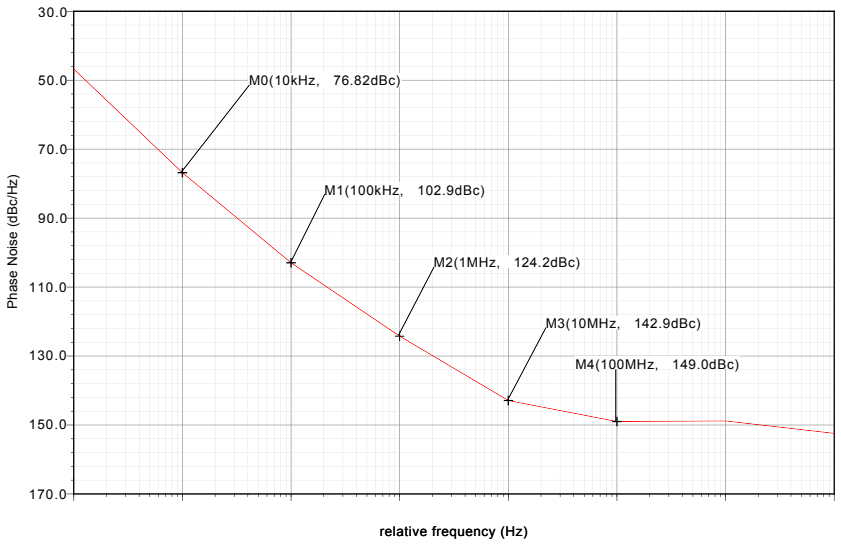

Figure 4.12: Post-layout phase noise simulation result of the DCO system in high-band maximum frequency.

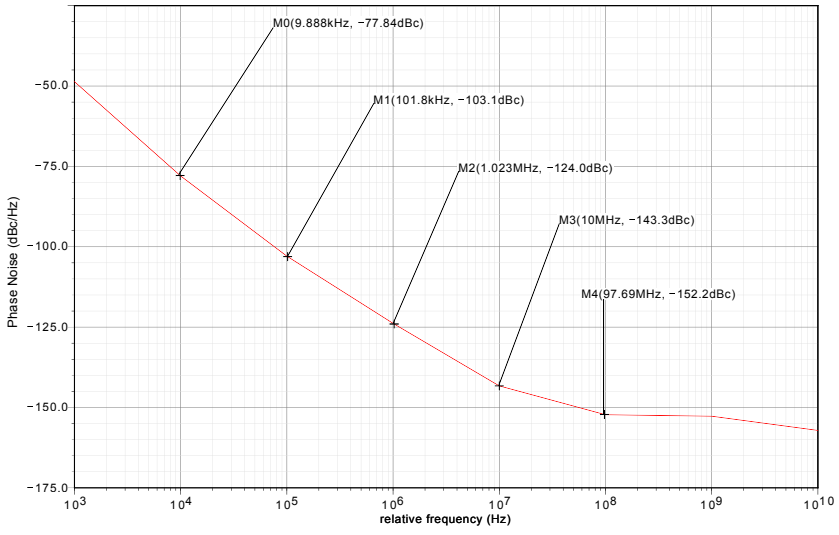

Figure 4.13: Post-layout phase noise simulation result of the DCO system in high-band minimum frequency.

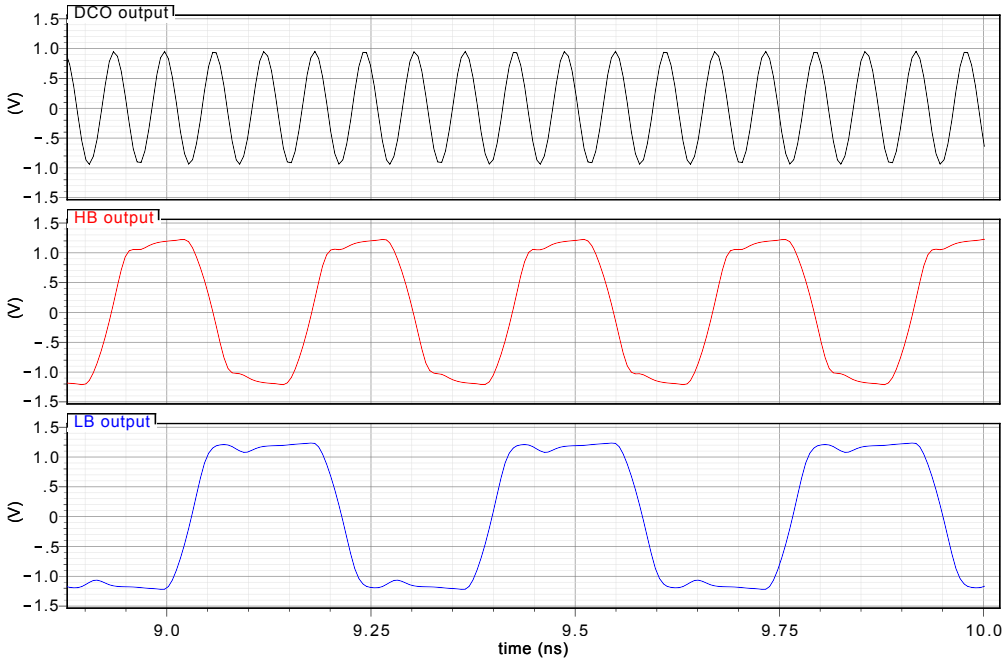

Figure 4.14: Transient Response of the DCO system outputs at DCO f_{max}

4.6 Figure of Merit

Figure of merit is used to determine the performance quality of a particular design. According to specific performance parameters in any design, a figure of merit can be mathematically defined. In designing an oscillator, phase noise, oscillation frequency and power consumption are among the most important parameters based on which any design is optimized and implemented. Equation 4.1 shows the figure of merit defined to specify the performance quality of an oscillator based on the design parameters [24].

$$FOM_1 = PN(\Delta f) - 20log\frac{f_0}{\Delta f} + 10log(\frac{P_{dc}}{1mW}) \tag{4.1}$$

where $PN(\Delta f)$ is the phase noise at offset frequency of Δf, f_0 is the central oscillation frequency and P_{dc} is the DC power consumption of the DCO core. According to the results derived in this chapter, a figure of merit of -186.8 dBc/Hz is calculated for the final DCO core design.

It is important to consider tuning range as an important design parameter that has to be included in figure of merit definition. Based on this, figure of merit 2 is defined to consider tuning range as an important performance factor which is defined in equation 4.2.

$$FOM_2 = FOM_1 - 20log(\frac{\%TR}{10}) \tag{4.2}$$

where TR is the tuning range of the DCO core and is defined in equation 2.12. FOM_2 for the final DCO core design is -198.8 dBc/Hz. Since the tuning range is much more than %10 (%40), FOM_2 shows quite an improvement compared to FOM_1.

4.7 Final Conclusion

The DCO design presented in this documented shows a different approach to traditional oscillator design. The main requirement which was based on a low-power ADPLL design for WiMAX application was the main consideration during the initial design steps. During frequency planning, different architectures were investigated in order to generate the required I/Q signals with pre-defined specifications for two frequency bands. The idea of doubling the DCO core frequency in order to have a single core LC oscillator was based on the idea of a low-power design. High frequency operation of the DCO and dividers and also the output phase noise requirements demanded the use of power hungry frequency dividers and buffers. The length of the dividing path with each block adding to the noise floor, total power consumption of this DCO system is increased to a value which was trying to be avoided in the first place.

FOM_1 in this design is comparable to many previous designs. On the other hand, the main specification for this design is the tuning range of the DCO core. This is the most important feature of the DCO which allows the whole system to operate and cover the two frequency bands with a single-core DCO. Therefore, FOM_2 is an important performance

assessment which shows how this design is different than the previous designs and publications.

Frequency Planning also demanded a unique I/Q signal generation by the dividers. A novel architecture is proposed to cover both frequency bands with desired output specifications and top-level layout considerations. Several changes were made to the dividing architecture due to the high frequency performance which disqualified the use of conventional flip-flop-based frequency dividers. Three main frequency dividing blocks and a digital frequency doubler were designed and laid out for this system.

4.7.1 Future Works

In order to use the proposed design in future transceiver architectures, two points have to be kept in mind:

1. Top level layout: All the designed blocks parasitic were extracted after layout and in some cases different iterations were made between the layouts and the schematics. The top level layout, however, requires more endeavor. The decoupling capacitors, bond wires and pads are among the important parts of the top-level layout

2. Although the proposed architecture can be useful in order to cover multiple frequency bands at the same time, in order to reduce the power consumption of the proposed system, different approaches such as switched inductor may be useful to decrease the DCO frequency and achieve the required phase noise with less power hungry frequency dividers and buffers.

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Appendix A

40 nm Technology Characteristics

In a high frequency design, it is important to be familiar with the intrinsic characteristics of different devices. Regarding MOS transistors, intrinsic parameters of the device play an important role in RF design.

- Transconductance efficiency g_m/I_D: in high frequency operation, it is desired to reach a certain transconductance gain (g_m) with minimum drain current (I_D). The ratio g_m/I_D can give insight for this particular characteristic. This ratio also defines the cut-off frequency of the device and determines the speed of the device.
- Cut-off frequency g_m/C_g: Wider devices provide larger transconductance gain with the price of a larger gate. The ratio g_m/C_g: is a suitable parameter in order to analyze this capability.
- Current density I_D/W: This ratio defines the current capability of the device. It can be used to characterize the current density as a function of length and be used to compare with other technologies.

Figures below show the simulation results for RF devices which are used in this design. No comparison is made to other technologies since no data is available.

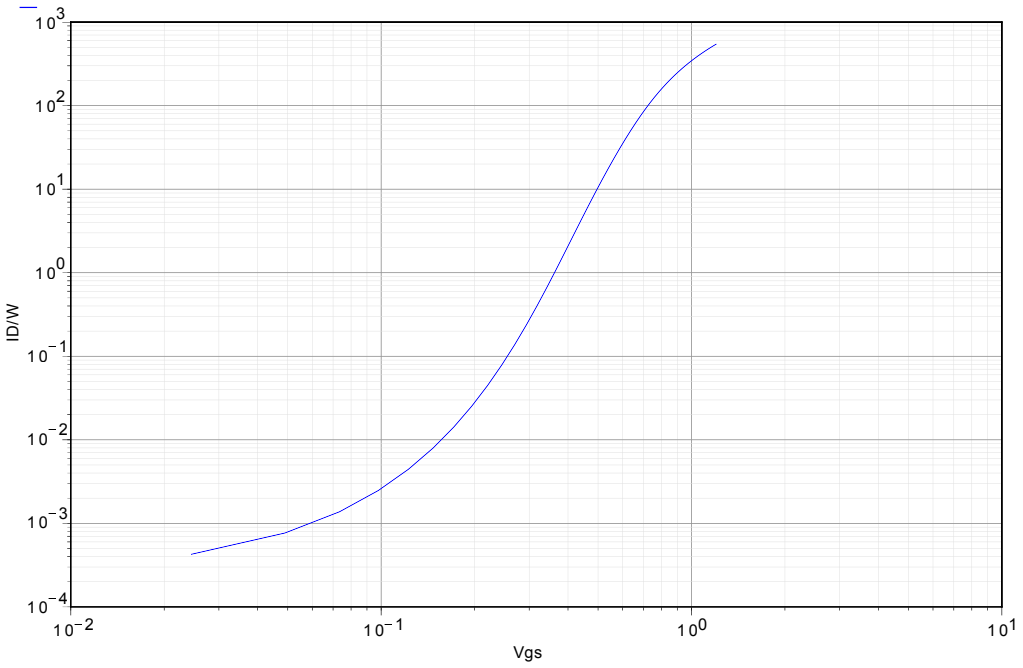

Figure A.1: Current density versus gate voltage ($V_D = 600\,mV$, $V_S = 0\,V$).

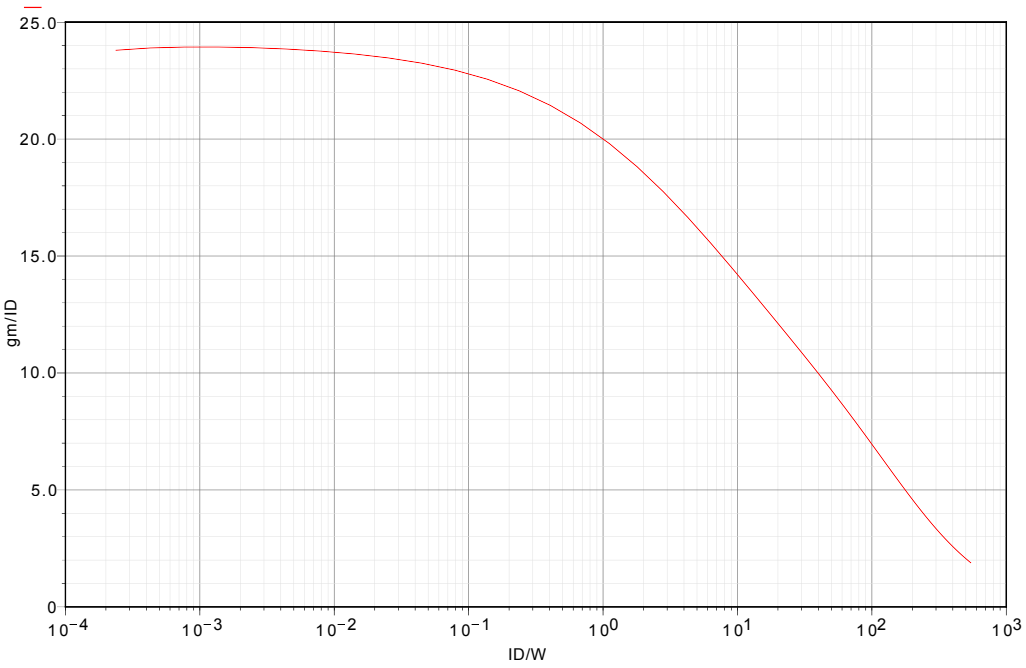

Figure A.2: Transconductance efficiency versus current density.

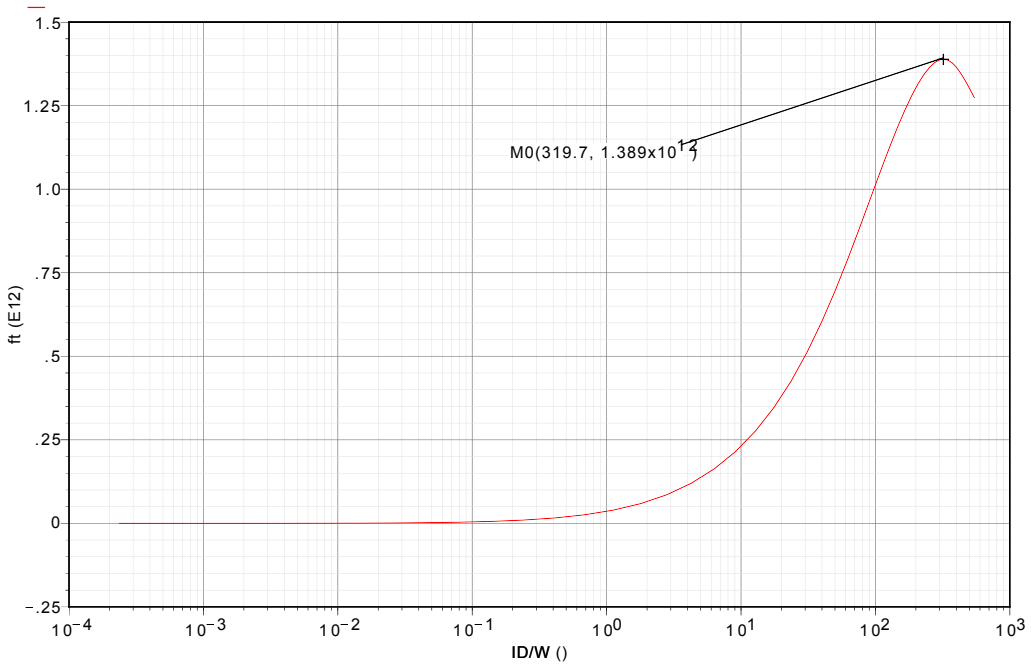

Figure A.3: Cut-off frequency versus current density.