Nearly 50 students from National Chiao-Tung University and National Tsing-Hua University and engineers from local industry (notably ICP plus, Realtek, Faraday, and ITRI) gathered at National Chiao-Tung University in Hsinchu Taiwan mid-afternoon on 30 March 2011 to hear Prof. Bogdan Staszewski of Delft University of Technology talk on “All-Digital RF Frequency Synthesis and Transmit Modulation.” An interactive and heated Q&A followed his lecture.

Dr. Staszewski described advanced studies on RF frequency synthesis and modulation technique for transmitters and briefly reviewed new progress on wide bandwidth all-digital phase-locked loops (ADPLLs) and software-defined PLLs.

As VLSI technologies advance to the nanometer CMOS arena, conventional charge-pump-based analog PLLs suffer from several problems, such as loop-filter leakage, limited dynamic range, and current matching problems, which may result in severer spur issues. Since ADPLLs can nevertheless circumvent these difficulties and realize true phase domain operation, they have recently spurred tremendous research efforts.

In a highly scaled CMOS technology, time resolution as determined by digital circuits may become superior to the voltage resolution of analog circuits under limited voltage headroom. In an ADPLL, phase error is detected by the time-to-digital converter (TDC), and the linear varactor in a conventional VCO is replaced by a varactor bank in a digitally controlled oscillator (DCO), which facilitates PVT tolerance, frequency acquisition, and phase tracking capability by multiband frequency tuning.

—Wei-Zen Chen
Chair, SSCS-Taipei

Abstract
One of the most important developments in the wireless industry within the last decade was the digitization of RF circuitry. This was in response to the incredible advancements of mainstream CMOS technology in both processing speed and circuit density, as well as the relentless push to reduce total solution costs through integration of RF, analog, and digital circuitry (Figure 1). Since the digital baseband part of a wireless communication channel has been traditionally implemented in the most advanced CMOS technology available at a given time for mass production, the need for single-chip CMOS integration has forced permanent changes to the way RF circuits are fundamentally designed. In this low-voltage nanometer-scale CMOS environment, high-performance RF circuits must exploit the time-domain design paradigm and heavily rely on digital assistance.

Thus, architecturally, the conventional analog-intensive PLL has been replaced with a novel ADPLL featuring a TDC and DCO. The ADPLL, combined with a novel digital power amplifier (DPA) that replaces the traditional analog-intensive power amplifier, has given rise to an all-digital polar transmitter (Figure 2). The conventional continuous-time analog-intensive receiver has been replaced with a novel direct-sampling discrete-time receiver that performs sophisticated filtering, such as FIR and IIR (Figure 1). As a result, RF transceivers based on this new approach now enjoy significant benefits of lower silicon area, cost, and power consumption over the traditional approaches and, consequently, they have become the architecture of choice for cellular phones.

The DCO (Figure 1), which performs RF frequency generation, consists of a large number (hundreds) of tiny binary-controlled varactors, whose step size is only 40 aF (atto-farads or 10E-18 farads). This is the smallest that the most advanced lithography
can create. Despite their miniscule size, their frequency step at the RF (2 GHz) output is as high as 10 kHz, which is too coarse for most wireless standards. The solution was to perform high-speed (100s of MHz) \( \Sigma \Delta \) dithering of the single varactor to obtain a much finer time-averaged fractional capacitance. The DCO is a form of an RF DAC, where the “analog” output is a frequency deviation. All traditional DAC design concerns, such as device matching, careful layout are applicable here. The DPA is also a form of an RF-DAC, where the “analog” output is an amplitude of the RF sinusoidal output. The amplitude is controlled by regulating the number of active MOS transistor switches by virtue of AND gates. Fine amplitude resolution is achieved also by \( \Sigma \Delta \) dithering.

**FIGURE 1:** Block diagram of a single-chip cellular phone radio based on the digital RF techniques. The only external components are the RF front-end module with the power amplifier and the battery management.

**FIGURE 2:** Conceptual diagram of an ADPLL-based transmitter.
The digital RF principles have been used at Texas Instruments (TI) to develop three generations of a Digital RF Processor (DRP): single-chip Bluetooth [1], GSM [2], and EDGE [3] radios realized in 130-nm, 90-nm, and 65-nm digital CMOS process technologies, respectively. Figure 3 shows the chip micrographs.

References


—Robert Bogdan Staszewski
TU Delft

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**CONGRATULATIONS NEW SENIORS**

*Fourteen Elected in April and June*

Kenneth Barnett  
Central Texas Section

Gene Brusche  
Philadelphia Section

Andrea Cathelin  
France Section

Craig Christensen  
Eastern Idaho Section

Ichiro Fujimori  
Orange County Section

Alexander Hoeffler  
Central Texas Section

Sergio Liberman  
Central Texas Section

Zheng Luo  
Central Texas Section

Pedram Mohseni  
Cleveland Section

Joachim Neves-Rodrigues  
Sweden Section

Peter Nilsson  
Sweden Section

Jonathan Strange  
U.K. and Republic of Ireland Section

Khurram Waheed  
Central Texas Section

Jeffrey Walling  
Princeton/Central Jersey Section

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