ET4371: "Digital RF"

				Office Hours
Lecturer:	R. Bogdan Staszewski	HB 18.270	R.B.Staszewski@tudelft.nl	Wed 13.00-14.00
Tutors:				
Lead	Iman Madadi	HB 18.280	I.Madadi@tudelft.nl	Wed 15.00-16.00
ADPLL	Augusto Ximenes	HB 18.280	A.R.Ximenes@tudelft.nl	Fri 14.00-15.00
TX/RX	Massoud Tohidian	HB 18.280	M.Tohidian@tudelft.nl	Fri 15.00-16.00

Lecture Timetable for 2012-2013 Fourth Semester (Q4)

Week	Lecture	Date		Room	Time	Tasks
4.1	1	Apr 23	Tue	TN Cl10 (A272)	10:45—12:45	
	2	Apr 25	Thu	TN Cl7 (A257)	15:45-17:45	Hw-1 assigned
4.2	Holiday	Apr 30	Tue	-	-	
	3*	May 2	Thu	TN Cl7 (A257)	15:45-17:45	Hw-2 assigned
4.3	4	May 7	Tue	TN Cl10 (A272)	10:45—12:45	
	Holiday	May 9	Thu	-	-	
4.4	5	May 14	Tue	TN Cl10 (A272)	10:45—12:45	Hw-3 assigned
	6	May 16	Thu	TN Cl7 (A257)		Project assigned
4.5	7	May 21	Tue	TN Cl10 (A272)	10:45—12:45	Hw-4 assigned
	8	May 23	Thu	TN Cl7 (A257)	15:45-17:45	
4.6	9	May 28	Tue	TN Cl10 (A272)	10:45—12:45	Hw-5 assigned
	10	May 30	Thu	TN Cl7 (A257)	15:45-17:45	
4.7	11*	Jun 4	Tue	TN Cl10 (A272)	10:45—12:45	Hw-6 assigned
	OFF	June 6	Thu	TN Cl7 (A257)	15:45-17:45	
4.8	12	Jun 11	Tue	TN Cl10 (A272)	10:45—12:45	
	Presentations	Jun 13	Thu	TN Cl7 (A257)	15:45-17:45	Project presentations
4.9	-	Jun 18	Tue	-	-	Project report due
4.10	-	Jun 25	Tue	-	-	~~Project report exam (approx. date)~~
4.11	Final exam (official)	Jul 4	Thu	CT-IZ 2.98	14:00-17:00	

Note: *Due to conference and travel, the May 2 lecture will be given by Wanghua Wu and on June 4 will be given by Iman Madadi and Massoud Tohidian.

Course Content

The past several years have successfully brought all-digital techniques to radio frequency (RF) synthesizers and transmitters, as well as digitally-intensive techniques to receivers. In addition, digital assistance is applied to RF circuits to improve performance and power consumption. This course will introduce basic concepts of the digital RF approach and walk through the major building blocks that comprise the new RF transceiver architecture:

1. All-digital phase-locked loop (ADPLL) comprising: digitally-controlled oscillator (DCO), time-to-digital converter (TDC), and digital loop filter.
2. All-digital transmitter featuring ADPLL with wideband modulation capability, and comprising digitally-controlled power amplifier (DPA)
3. Direct-sampling discrete-time receiver comprising switched-cap circuits that perform various FIR and IIR filter operations.

Homework exercises use Matlab to model and simulate the above three subsystems.

Lecture Outline

Twelve lectures will give the following exposure to the three main topics: (1) ADPLL: 7 lectures; (2) DPA: 2 lectures; (3) discrete-time RX: 3 lectures; in addition to an introduction and special topic lectures.

1 Introduction to the topics of digital RF and digitally-assisted RF
2 Digitally-controlled oscillator (DCO), its phase noise modeling and simulation
3 DCO interface: sigma-delta modulation, dynamic element matching, DCO gain normalization
4 Principles of phase-domain frequency synthesis: all-digital PLL (ADPLL)
5 Time-to-digital converter (TDC) and metastability
6 ADPLL closed-loop behavior
7 Direct frequency modulation of ADPLL
8 Principles of switched-mode and digital power amplifier (DPA)
9 DPA modeling and non-linearities; predistortion
10 Principles of a discrete-time (DT) receiver
11 Signal processing of a DT mixer: IIR, FIR and decimation
12 DT receiver modeling and simulation
13 Special topics, project presentations, etc.

Expected Prior Knowledge

Basic signal processing; basic knowledge of Matlab.

Literature and Study Materials

R. B. Staszewski and P. T. Balsara, *All-Digital Frequency Synthesizer in Deep-Submicron CMOS*, New Jersey: John Wiley & Sons, Inc., Sept. 2006. ISBN: 978-0471772552.

Also: IEEE Journal of Solid-State Circuits (JSSC), Transactions on Circuits and Systems (TCAS) and proceedings of ISSCC Conference and RFIC Symposium.

Homework: 40% Weight

Six homework assignments typically given out on the first class of the week (i.e., Tuesday) and **due within a 7-day week** (i.e., next Tuesday). Combination of problem questions and Matlab projects.

Final Project – Journal paper reading assignment: 20% Weight

Individual study of an IEEE JSCC paper chosen from a list. Approximately one month given to prepare a class presentation and report.

Final Examination: 40% Weight

Regularly scheduled closed-book final examination.